Bitland Confidential

V200HR M/B Schematics Document

2012-2-28

REV:1.2

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Cover Page	
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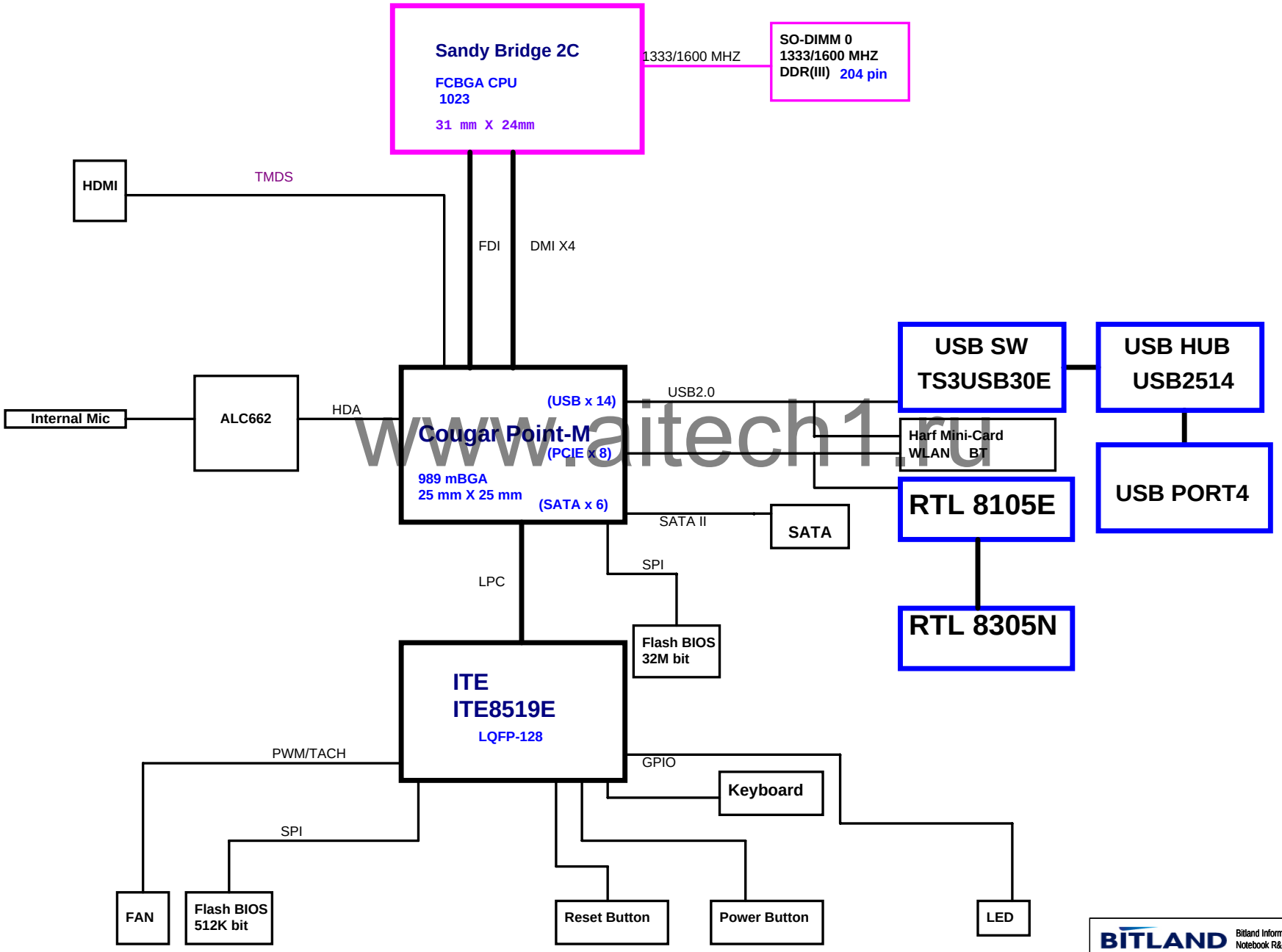

BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: Block Diagram

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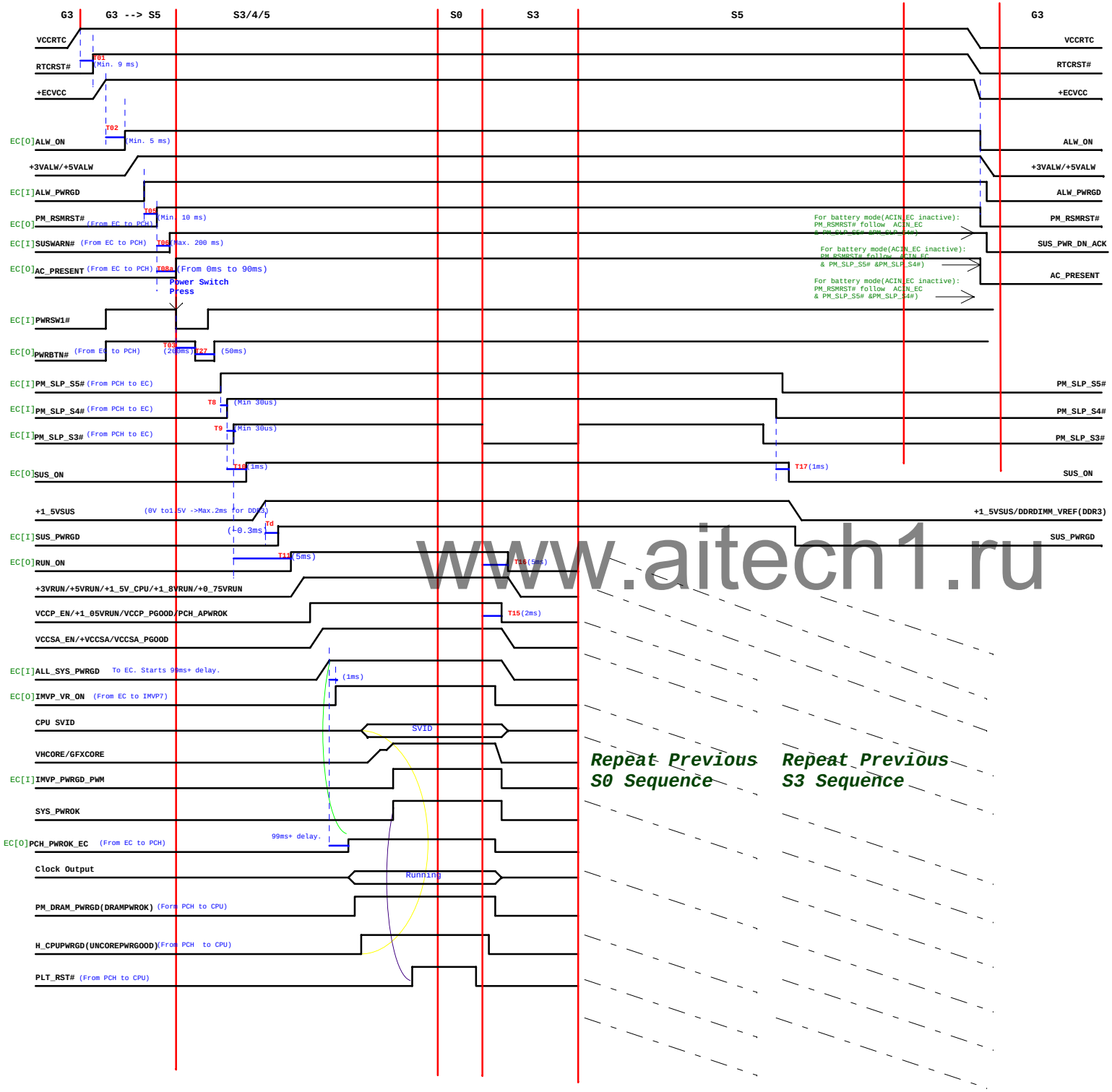

BITLAND	Bitland Information Technology Co.,Ltd. Notebook R&D Division	
Title: FAN/Thermal		
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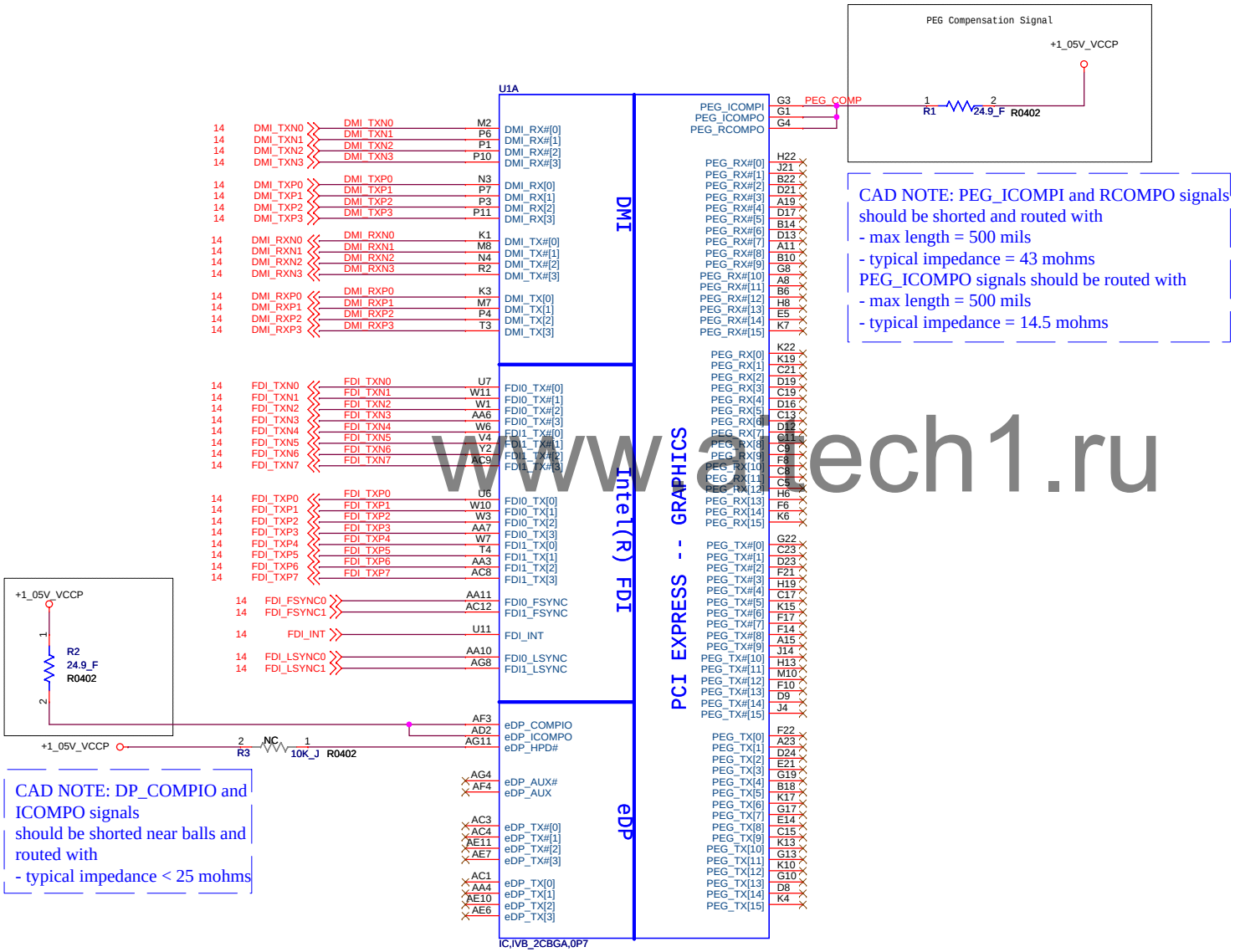
SANDYBRIDGE 2C BGA PROCESSOR (DMI,DP,PEG,FDI)



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	CPU (DMI,DP,PEG,FDI)		
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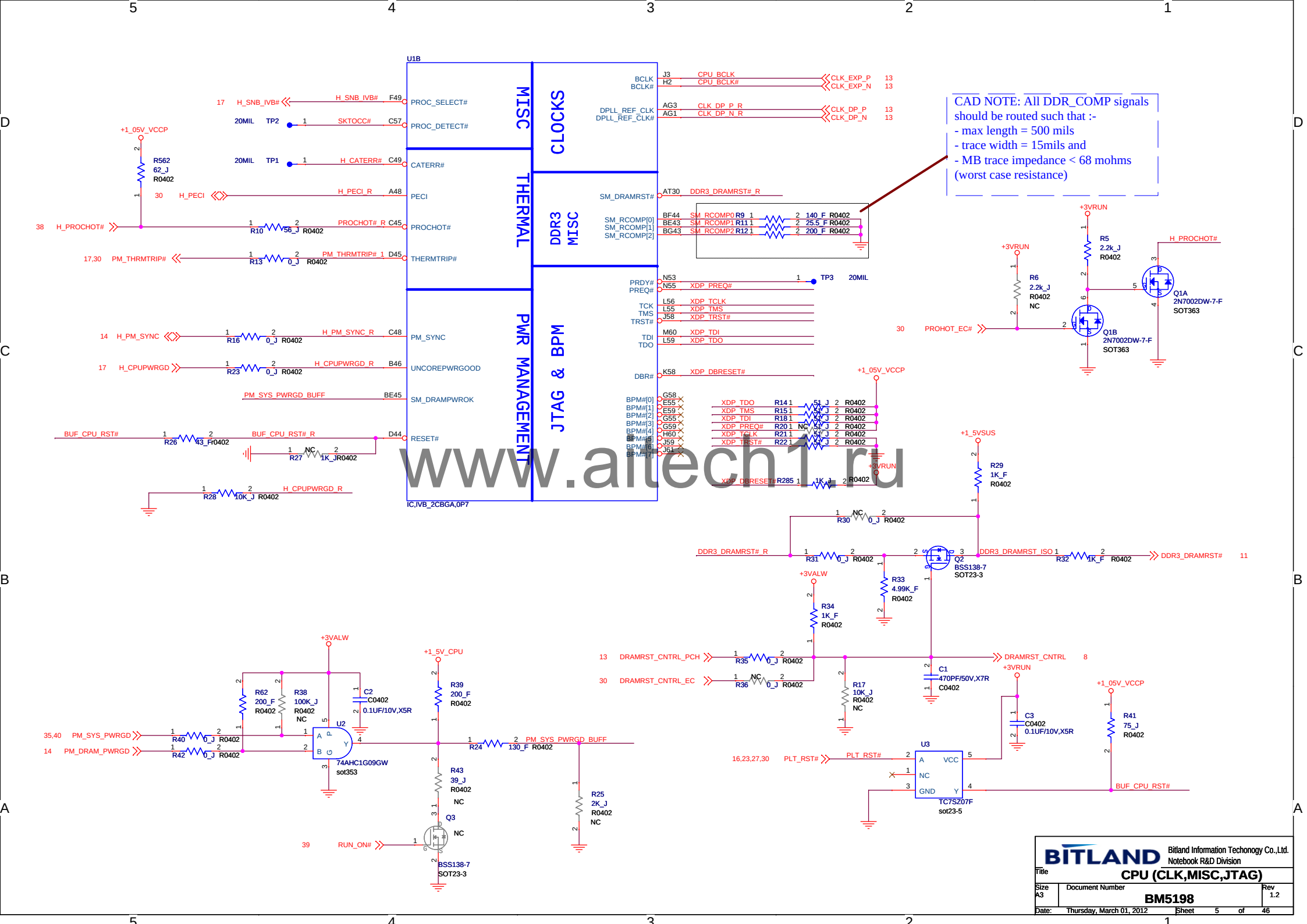
U1B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
PROC_SELECT#
PROC_DETECT#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
IC,IVB_2CBGA,0P7
CAD NOTE: All DDR_COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms
(worst case resistance)
Q1A 2N7002DW-7-F SOT363
Q1B 2N7002DW-7-F SOT363
Q2 BSS138-7 SOT23-3
Q3 NC BSS138-7 SOT23-3
U2 74AHC1G09GW sot353
U3 TC7SZ07F sot23-5
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BITLAND
Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division
Title
CPU (CLK,MISC,JTAG)
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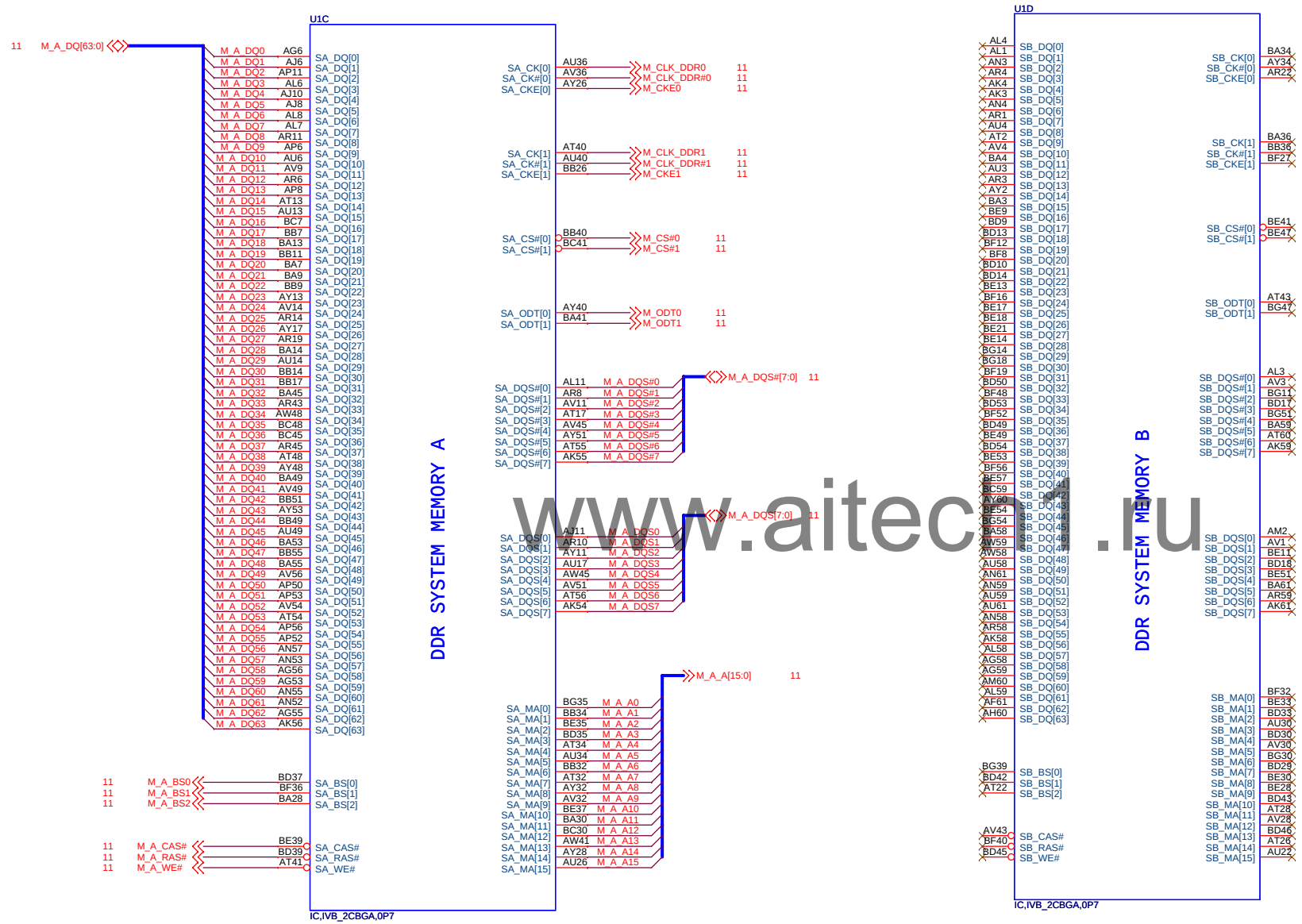

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Title	CPU (DDR3)	
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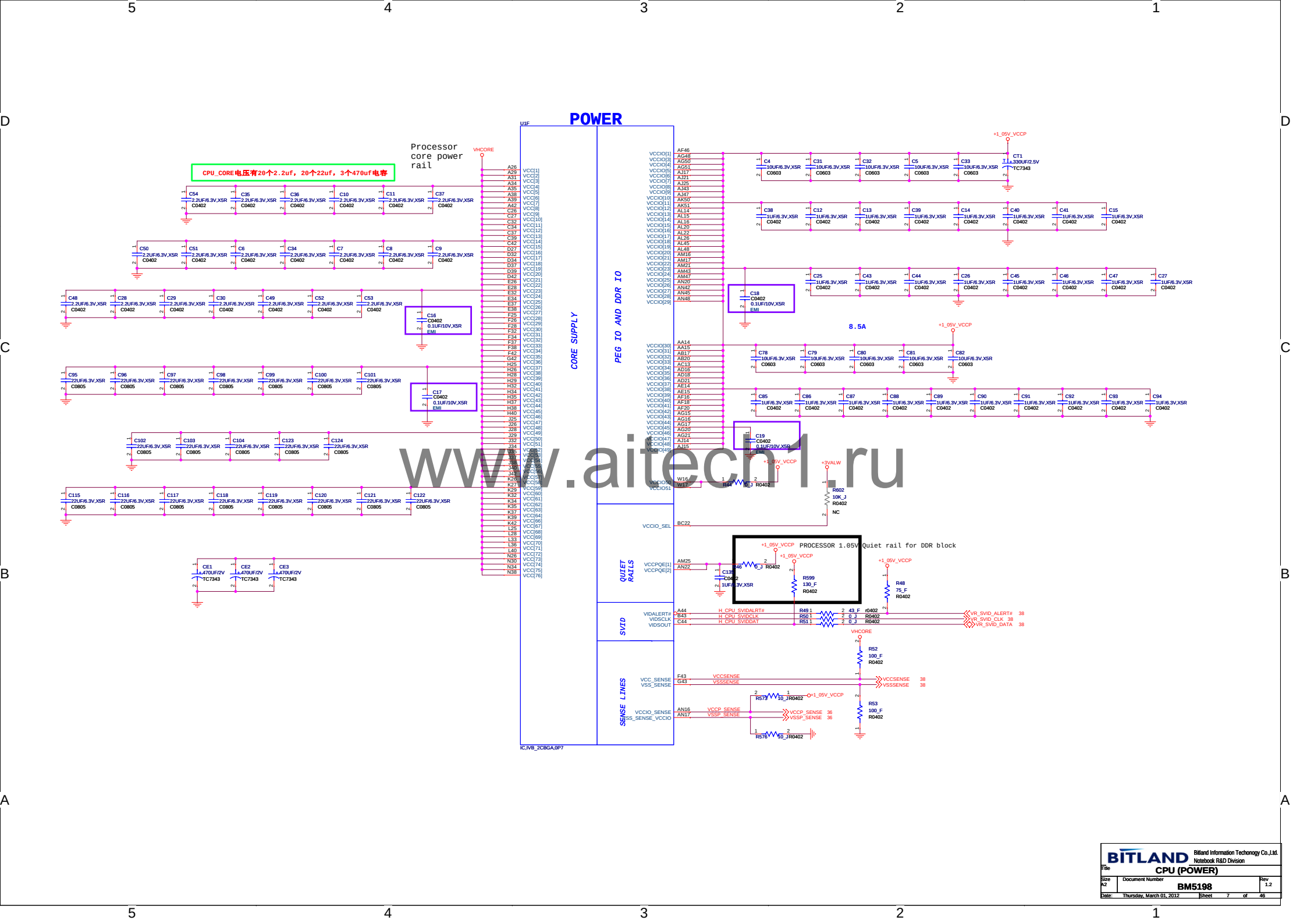

Title	CPU (POWER)		
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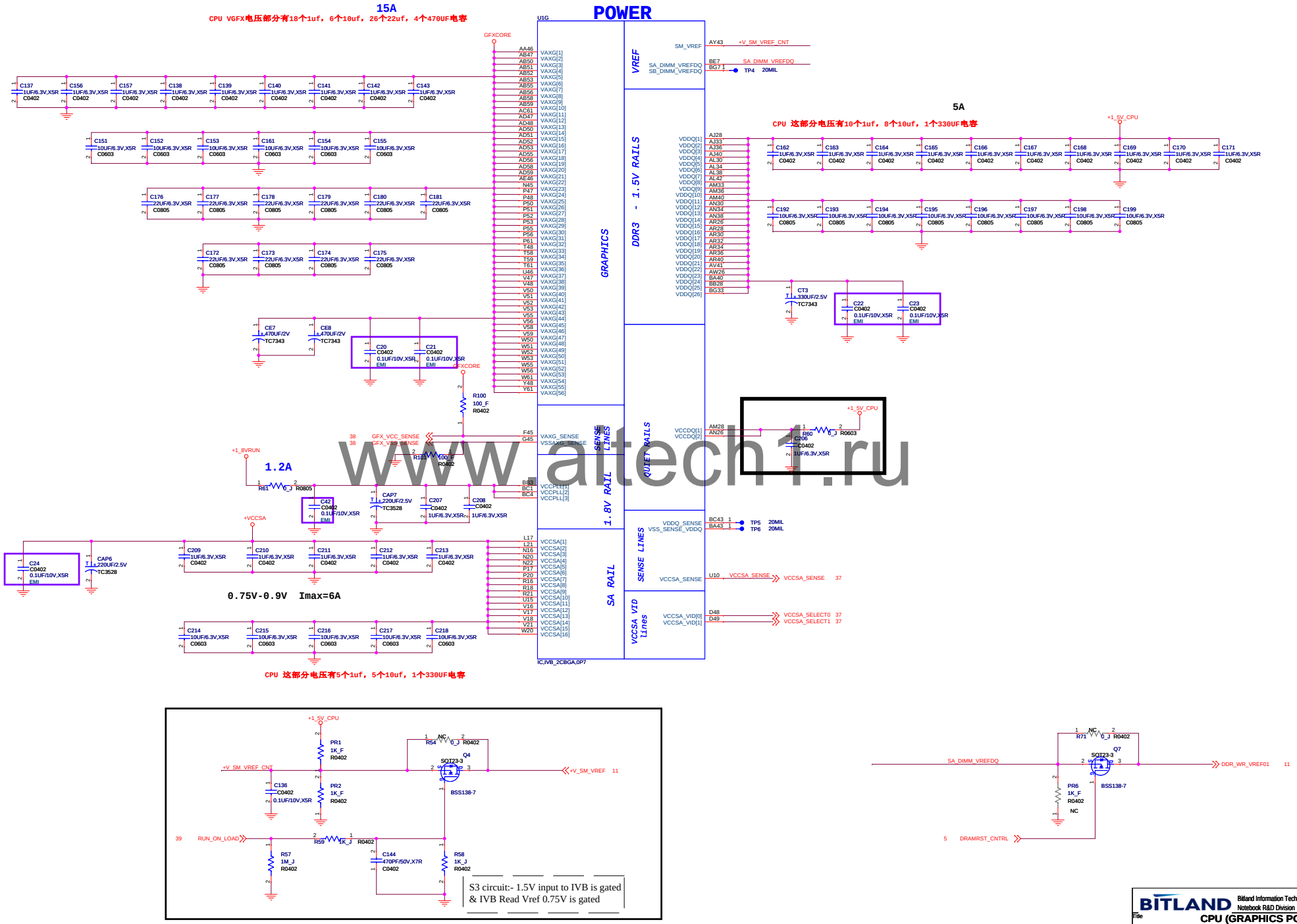
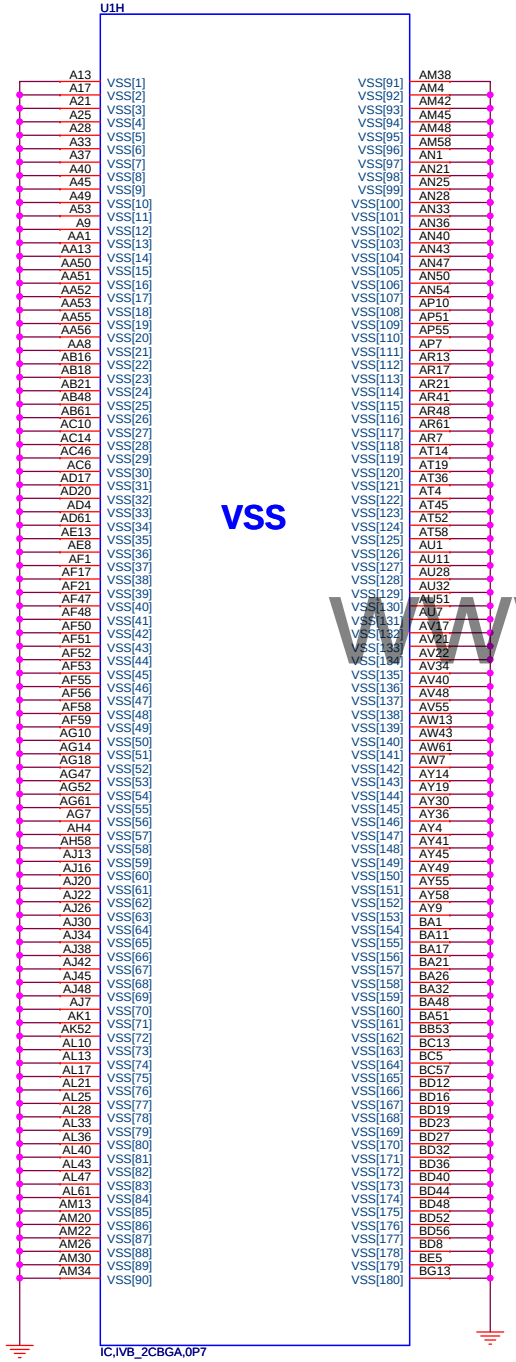
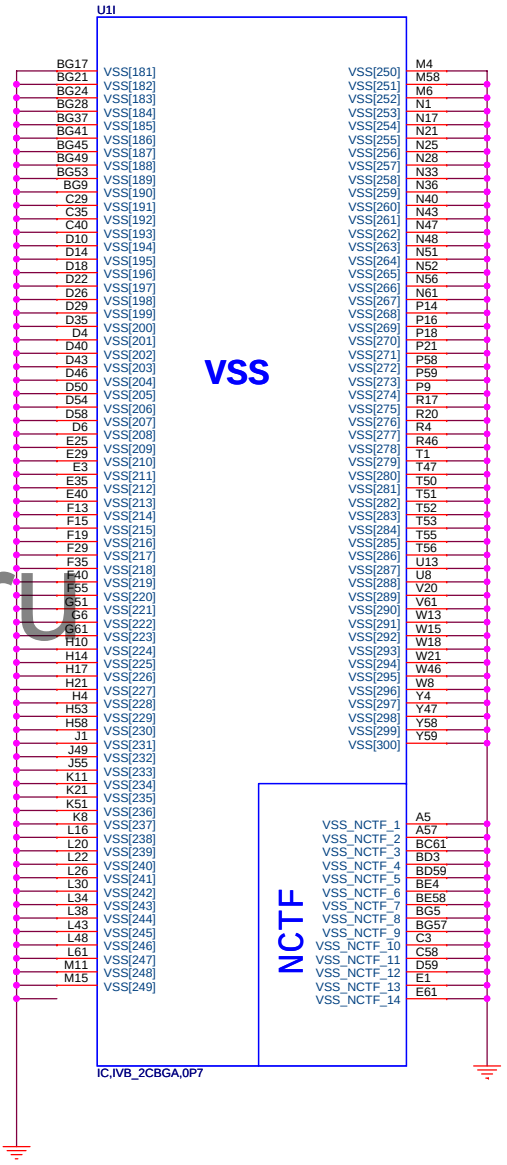
Notebook R&D Division







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Title	CPU (GND)		
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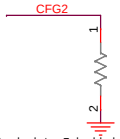
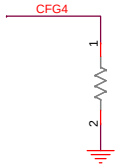
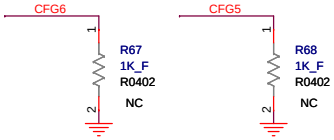
CFG2 1:(Default) Normal Operation; Lane # definition matches socket pin map definition
CFG2 0:Lane Reversed



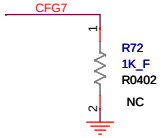
CGF4 1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port
CGF4 0:Enabled; An external Display Port device is connected to the Embedded Display Port

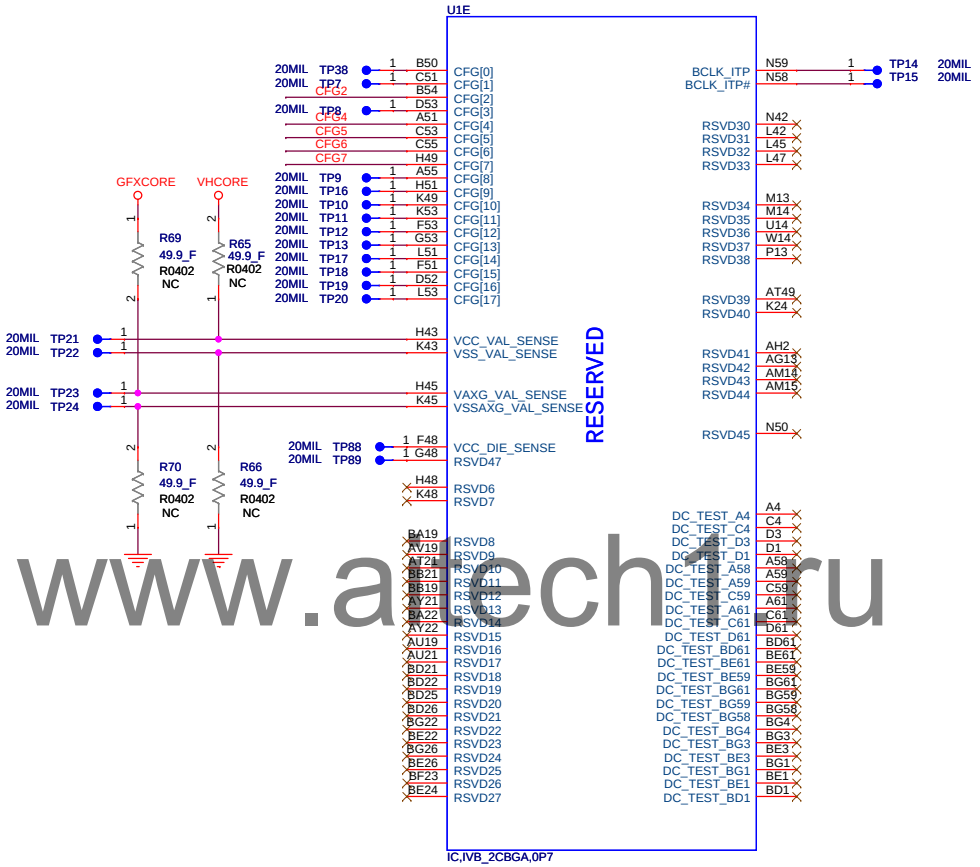


CGF[6: 5]
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



CFG7 1: (Default) PEG Train immediately following xxRESETB de assertion
CFG7 0: PEG Wait for BIOS for training





Title	CPU (RESERVED)
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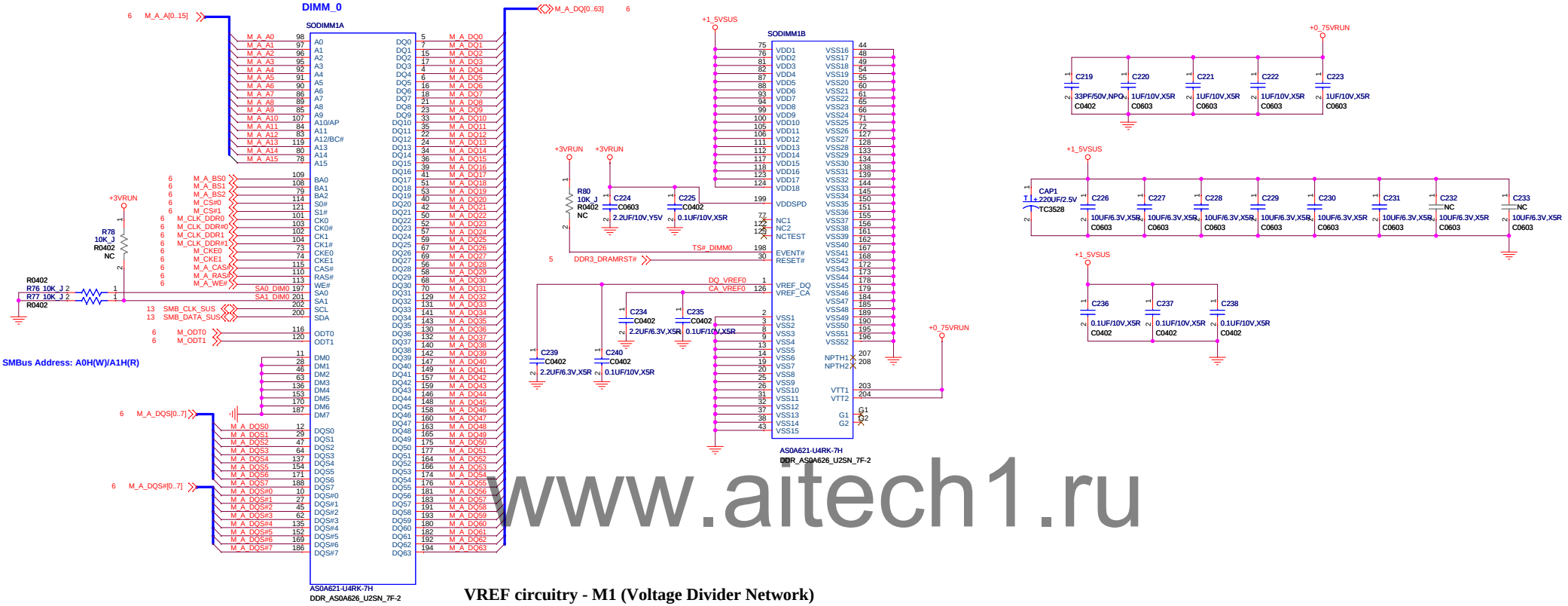
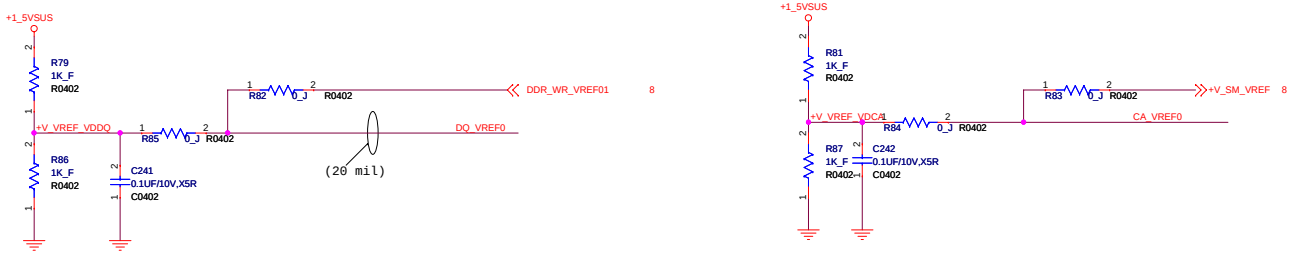


VREF circuitry - M1 (Voltage Divider Network) & M3 (Driven By Processor) implementation

M3+M1: Default Recommendation
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off state
M3: VREF_DQ driven by Processor



CAD NOTE:All VREF traces should be at least 20 mils wide and 20 mils spacing to other signals/planes

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Title: DDR3 SO-DIMM_0

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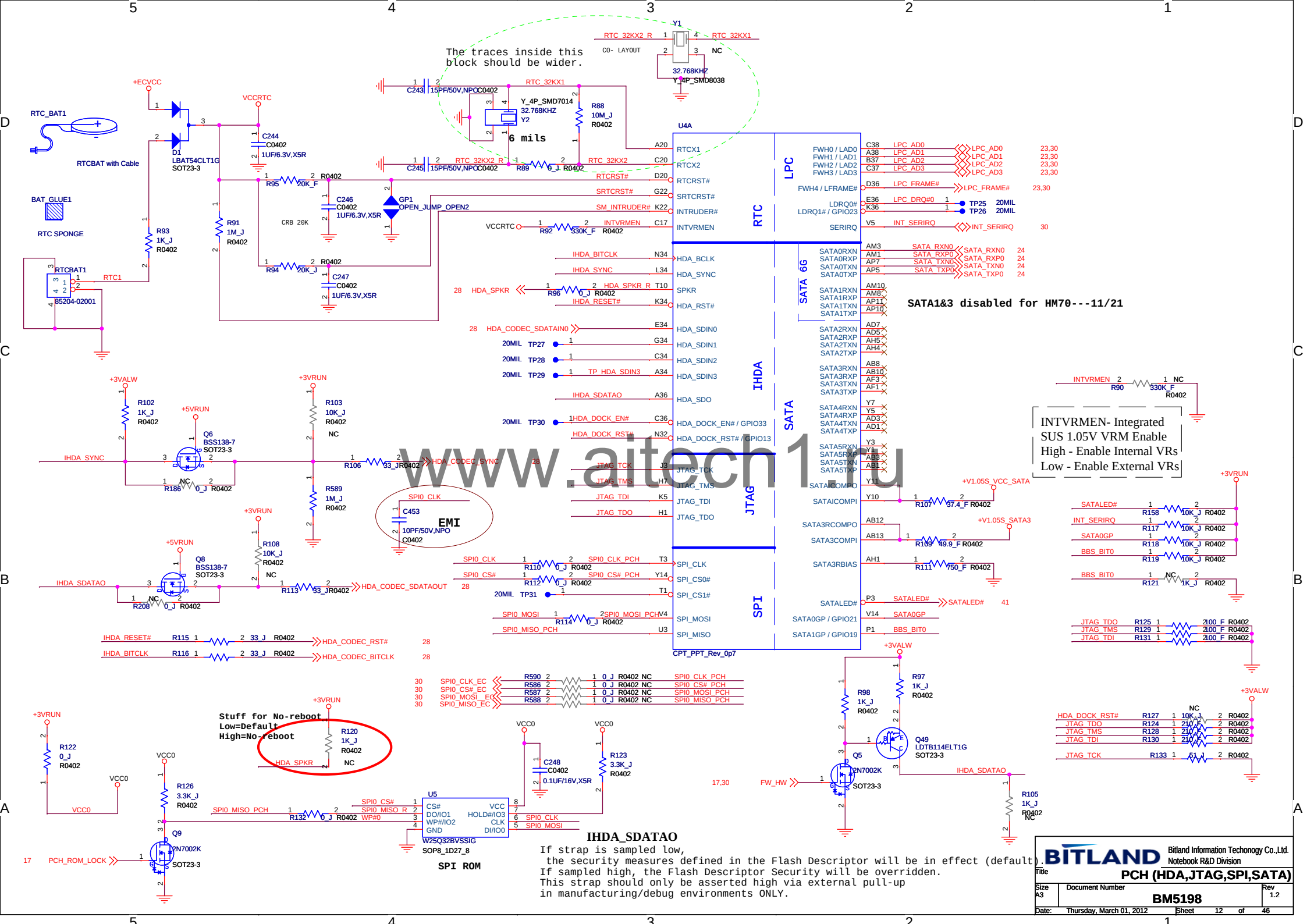
The traces inside this block should be wider.
6 mils
RTCBAT with Cable
RTC SPONGE
RTCBAT1
85204-02001
LBAT54CLT1G
SOT23-3
U4A
RTC
LPC
SATA 6G
IHDA
SATA
JTAG
SPI
CPT_PPT_Rev_0p7
SATA1&3 disabled for HM70---11/21
INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs
EMI
Stuff for No-reboot
Low=Default
High=No-reboot
SPI ROM
W25Q32BVSSIG
SOP8_1D27_8
IHDA_SDATAO
If strap is sampled low,
the security measures defined in the Flash Descriptor will be in effect (default).
If sampled high, the Flash Descriptor Security will be overridden.
This strap should only be asserted high via external pull-up
in manufacturing/debug environments ONLY.
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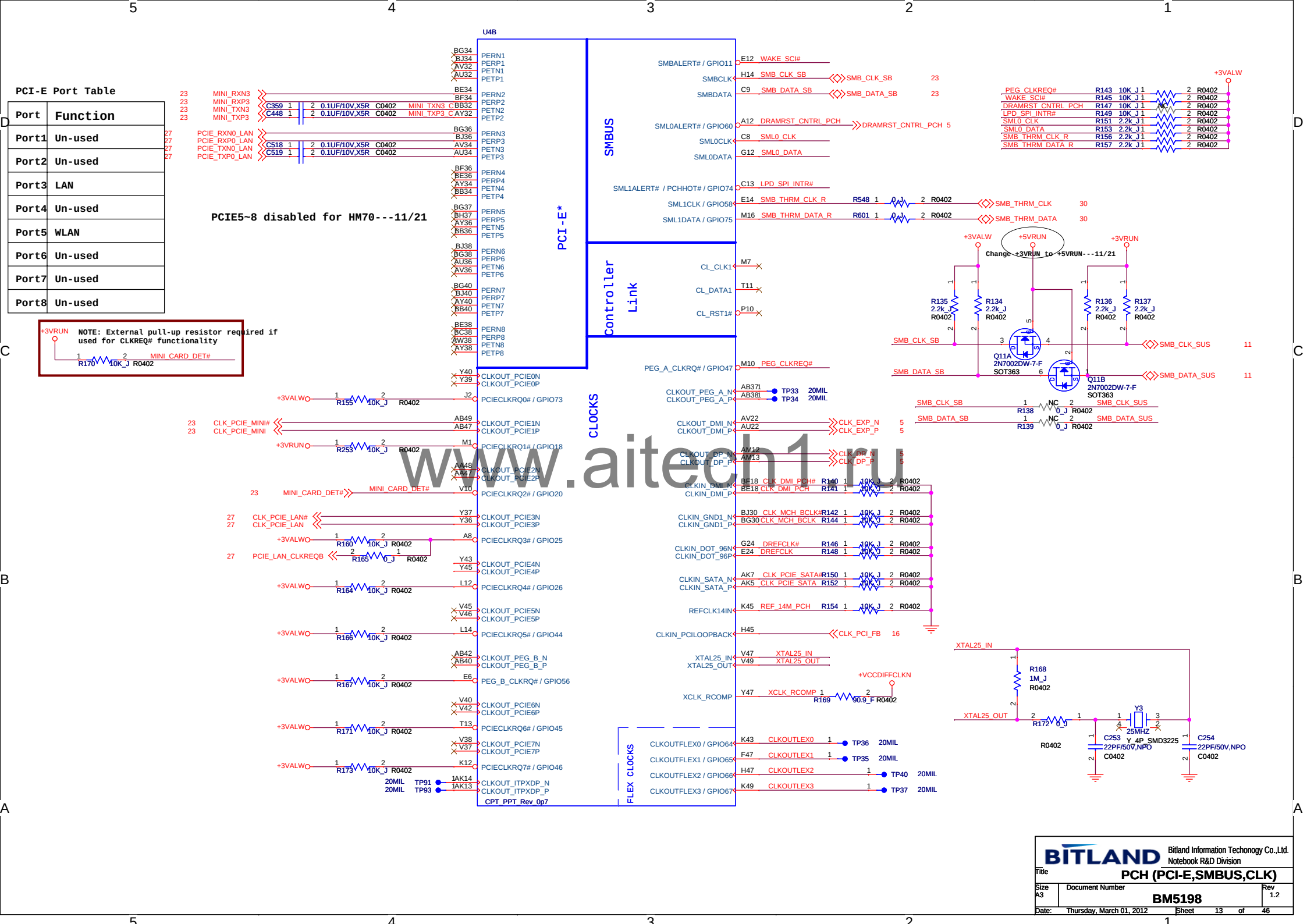
Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division
PCH (HDA,JTAG,SPI,SATA)
BM5198
Thursday, March 01, 2012

PCI-E Port Table

Port	Function
Port1	Un-used
Port2	Un-used
Port3	LAN
Port4	Un-used
Port5	WLAN
Port6	Un-used
Port7	Un-used
Port8	Un-used

PCIE5~8 disabled for HM70---11/21

NOTE: External pull-up resistor required if used for CLKREQ# functionality



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	PCH (PCI-E,SMBUS,CLK)		
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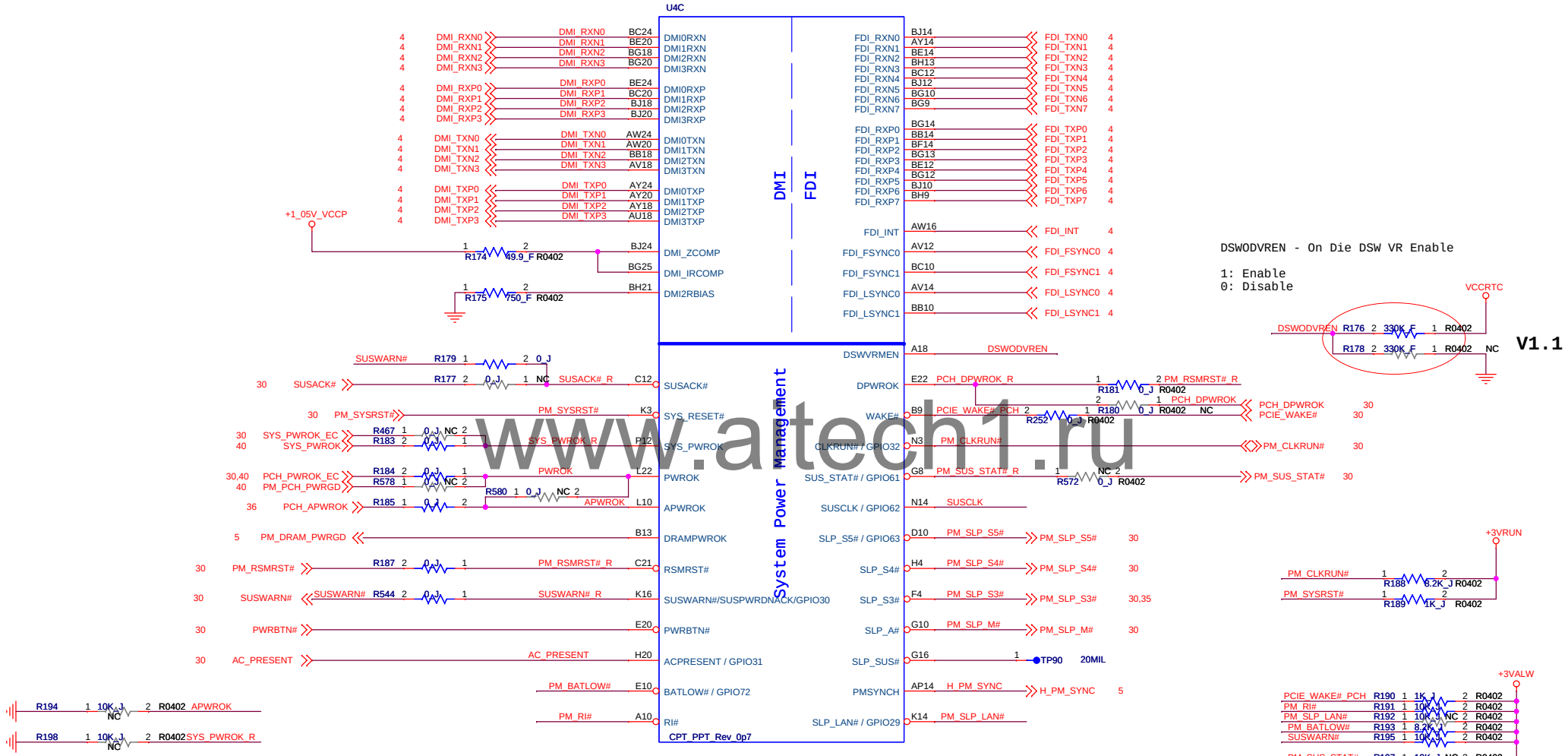

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	PCH (DMI,FDI,GPIO)		
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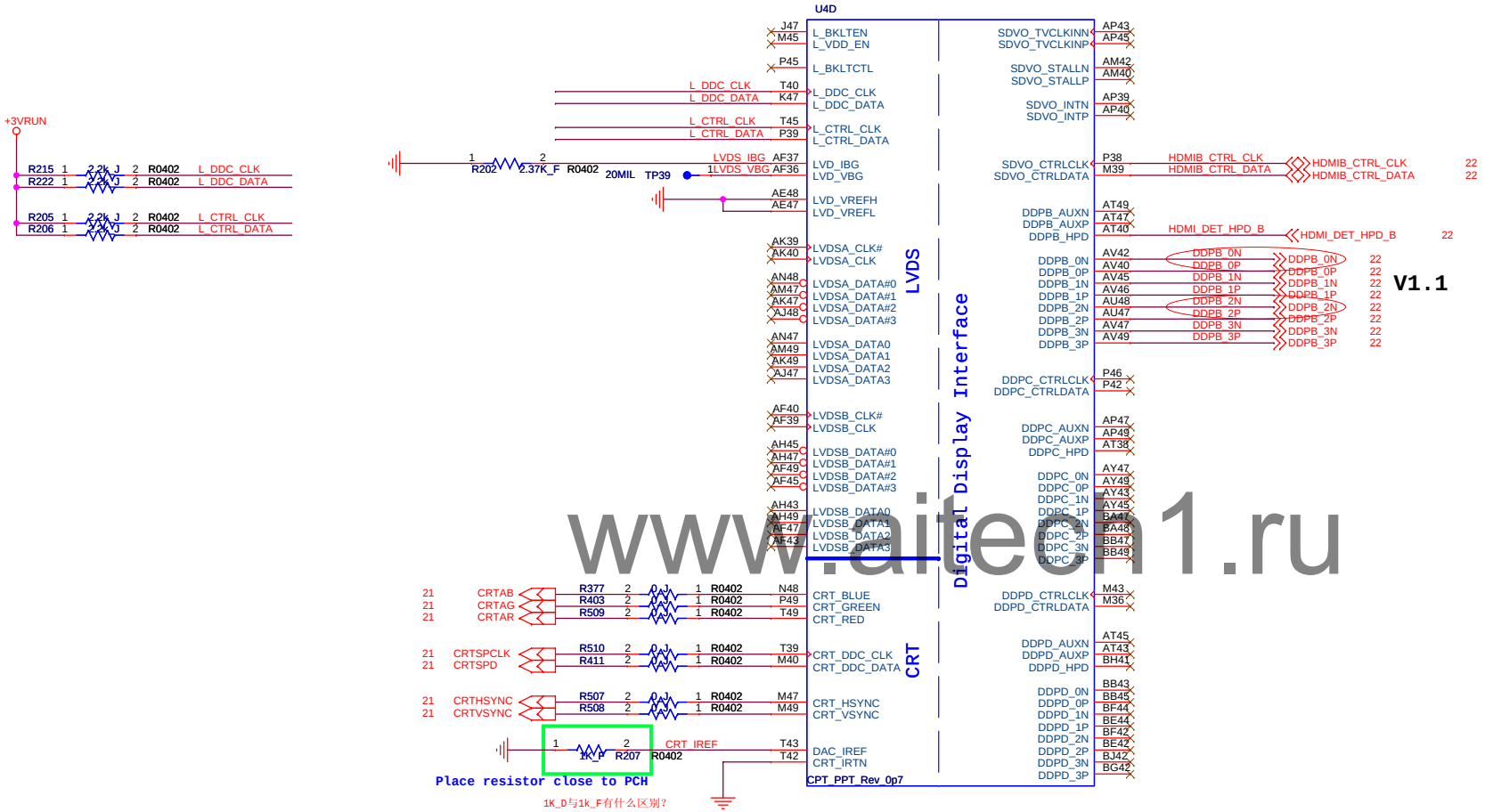

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	PCH (LVDS,DDI)		
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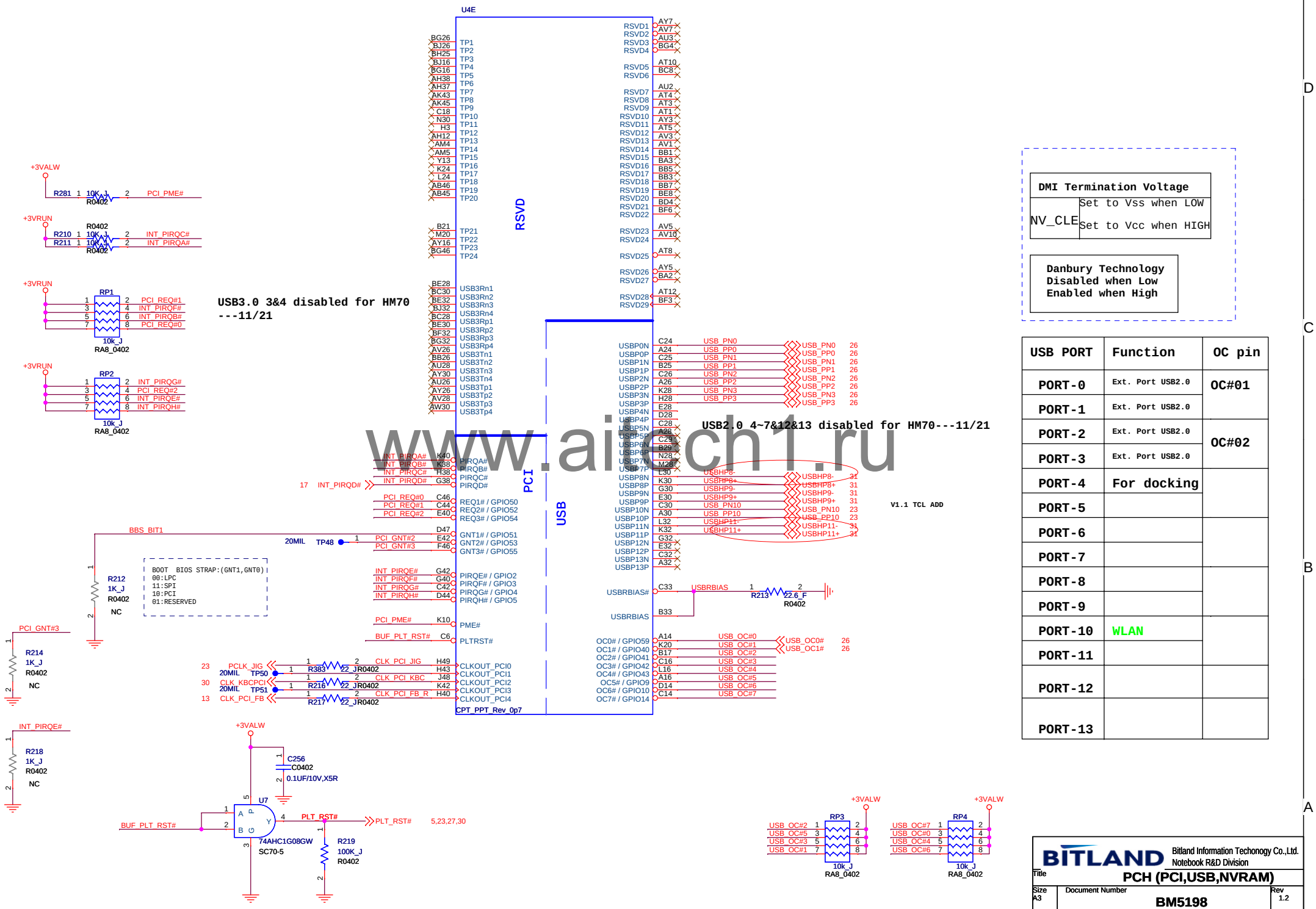

USB PORT	Function	OC pin
PORT-0	Ext. Port USB2.0	OC#01
PORT-1	Ext. Port USB2.0	
PORT-2	Ext. Port USB2.0	OC#02
PORT-3	Ext. Port USB2.0	
PORT-4	For docking	
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9		
PORT-10	WLAN	
PORT-11		
PORT-12		
PORT-13		

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Title: PCH (PCI,USB,NVRAM)

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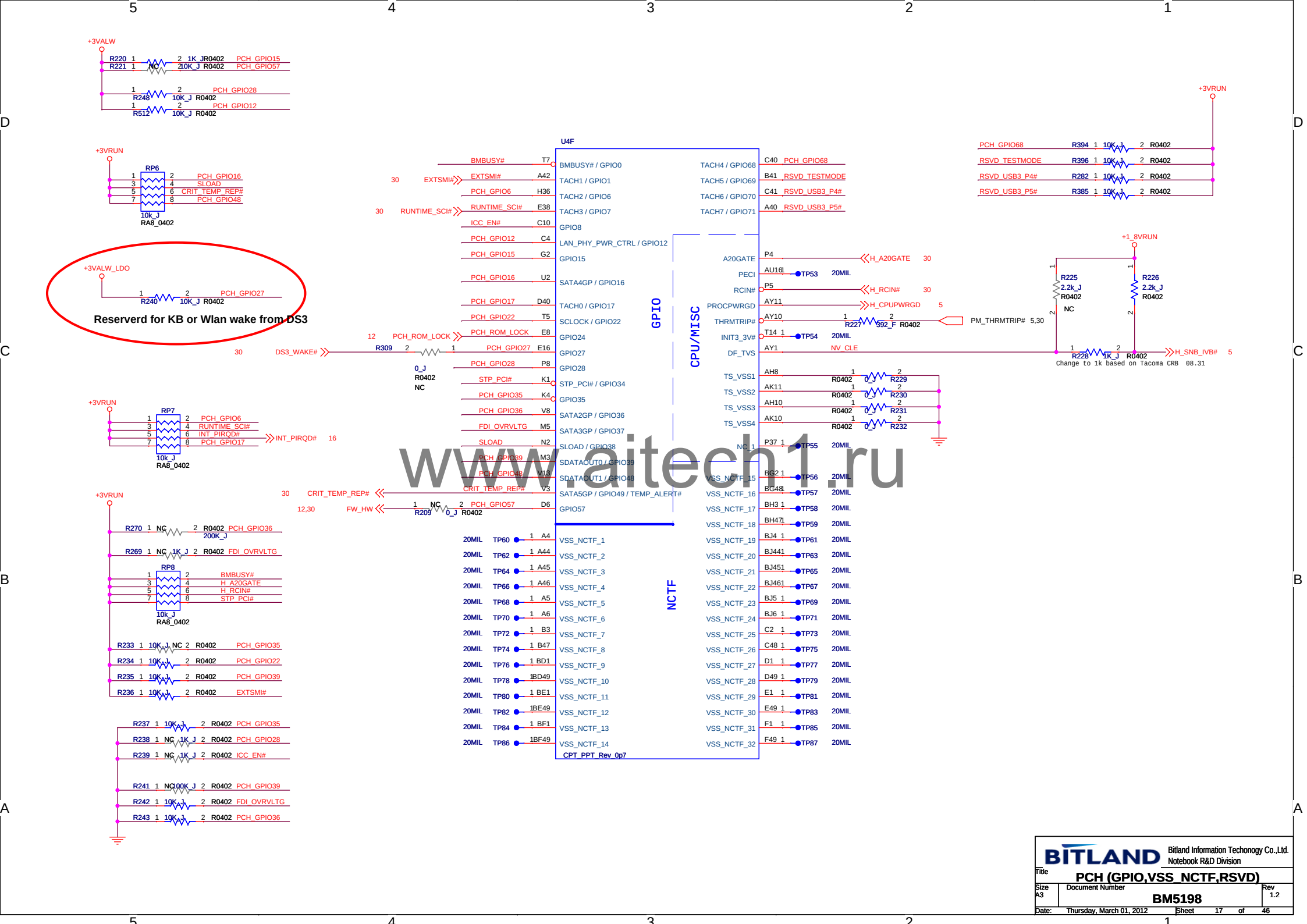

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Title	PCH (GPIO,VSS_NCTF,RSVD)		
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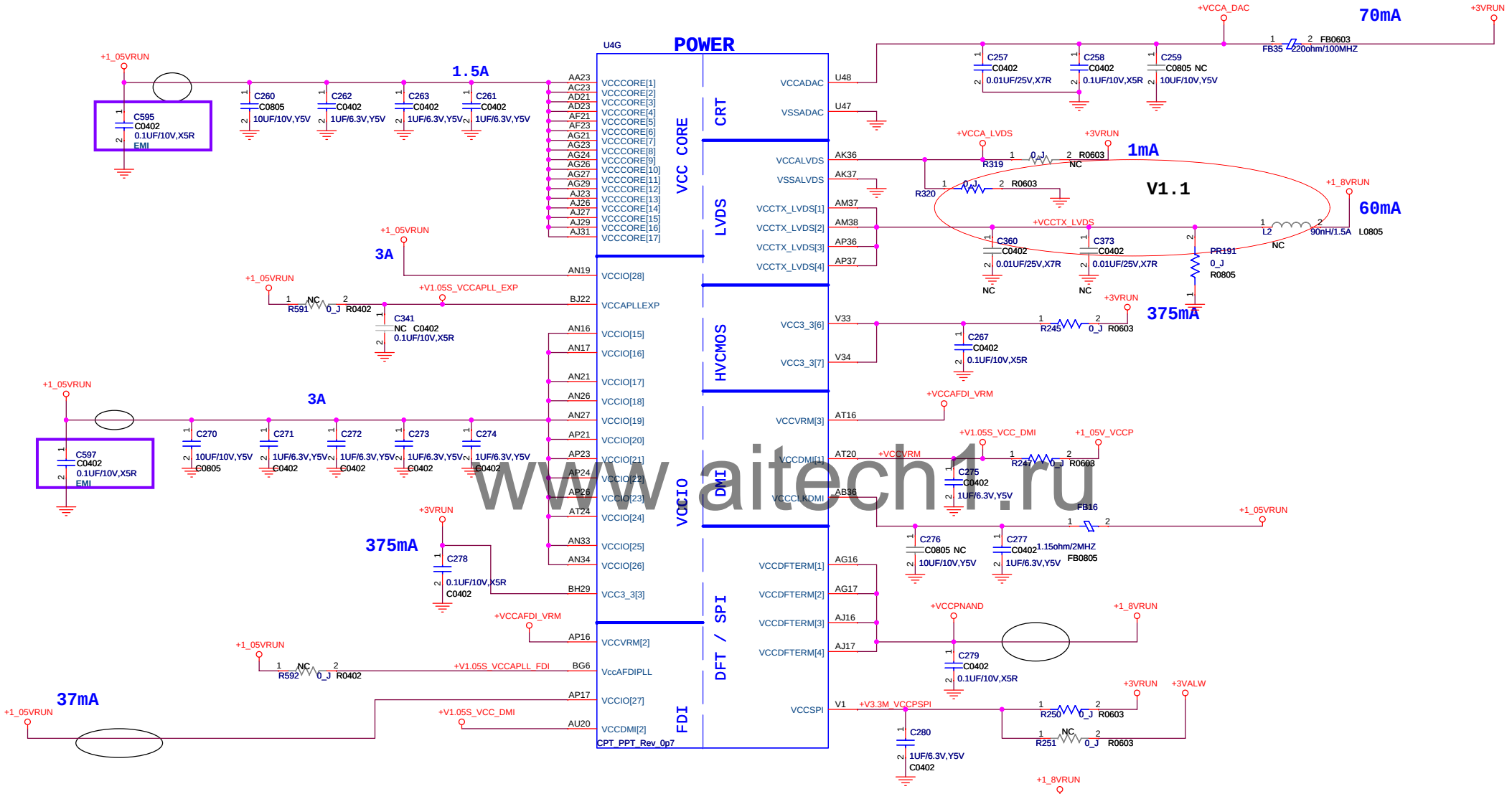

Company	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	PCH (POWER1/2)
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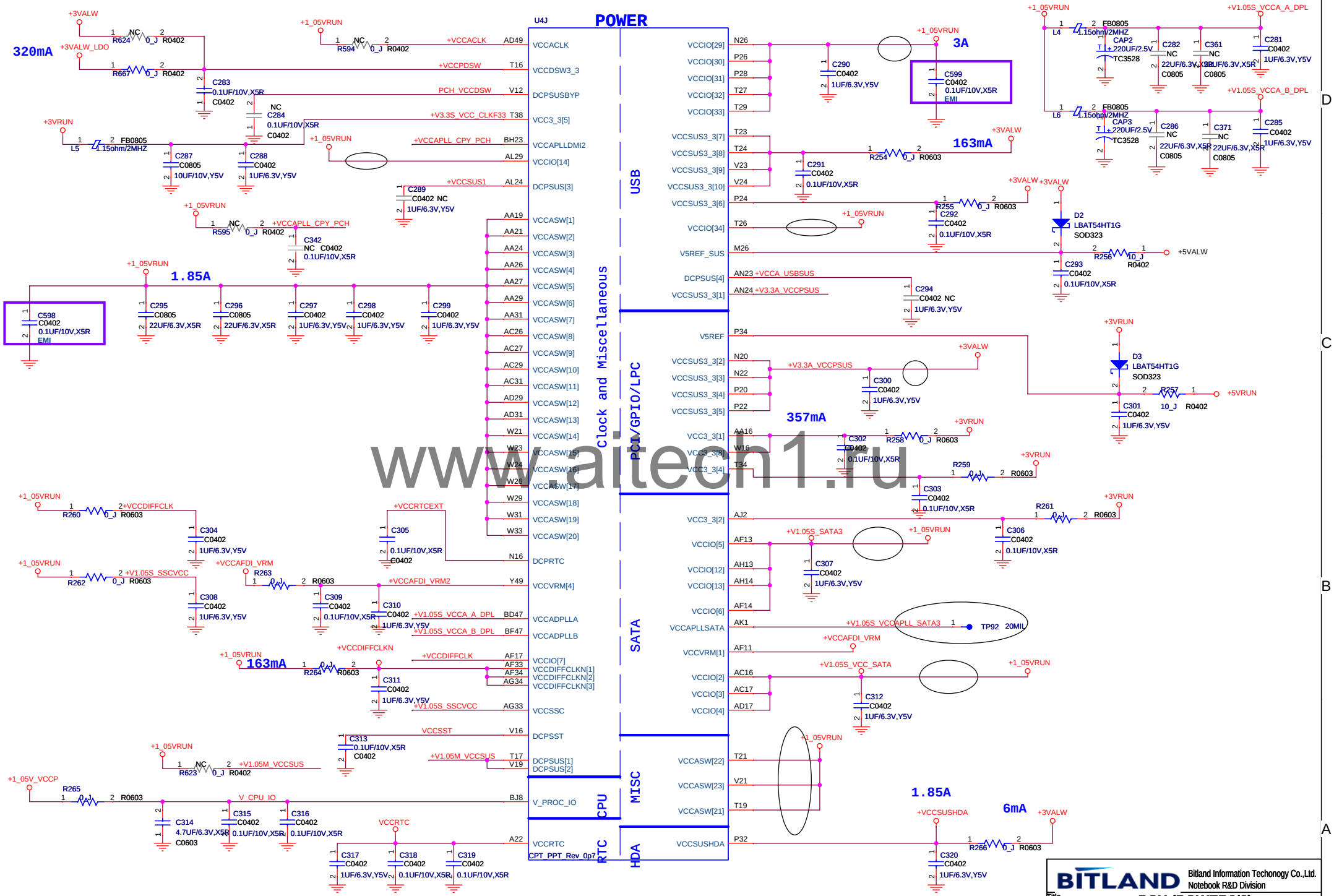

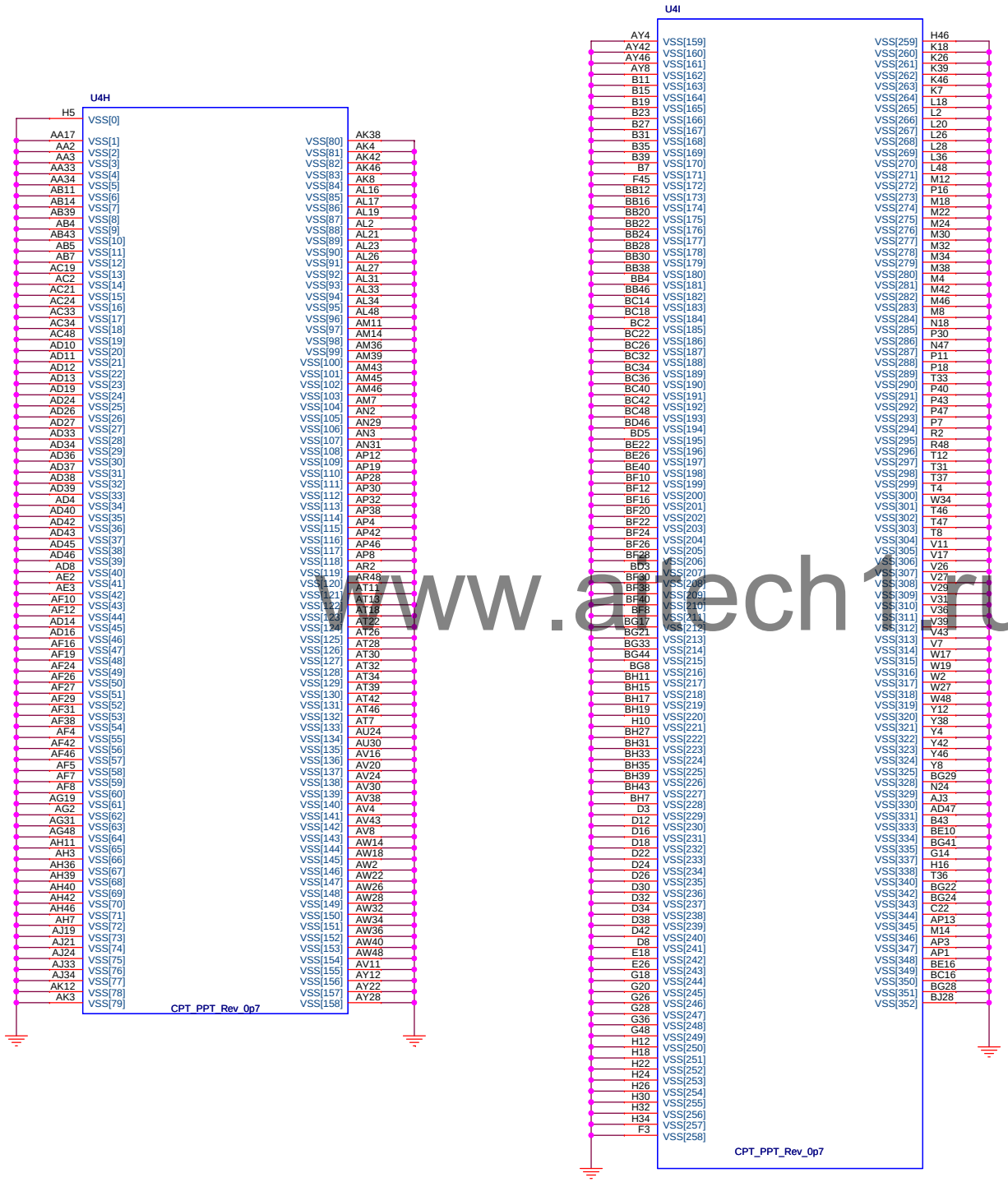

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Title: PCH (GND)

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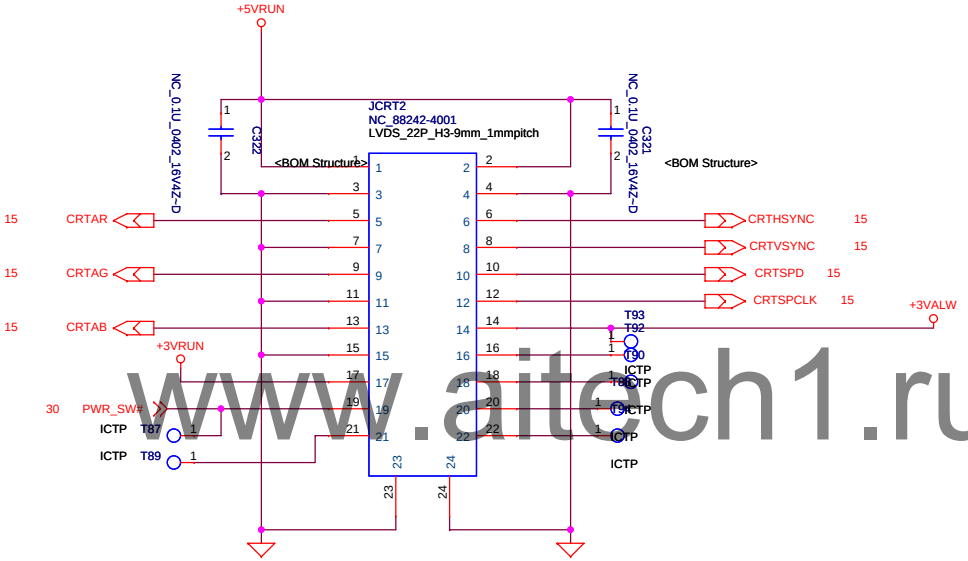

add vga connector

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Title: CRT		
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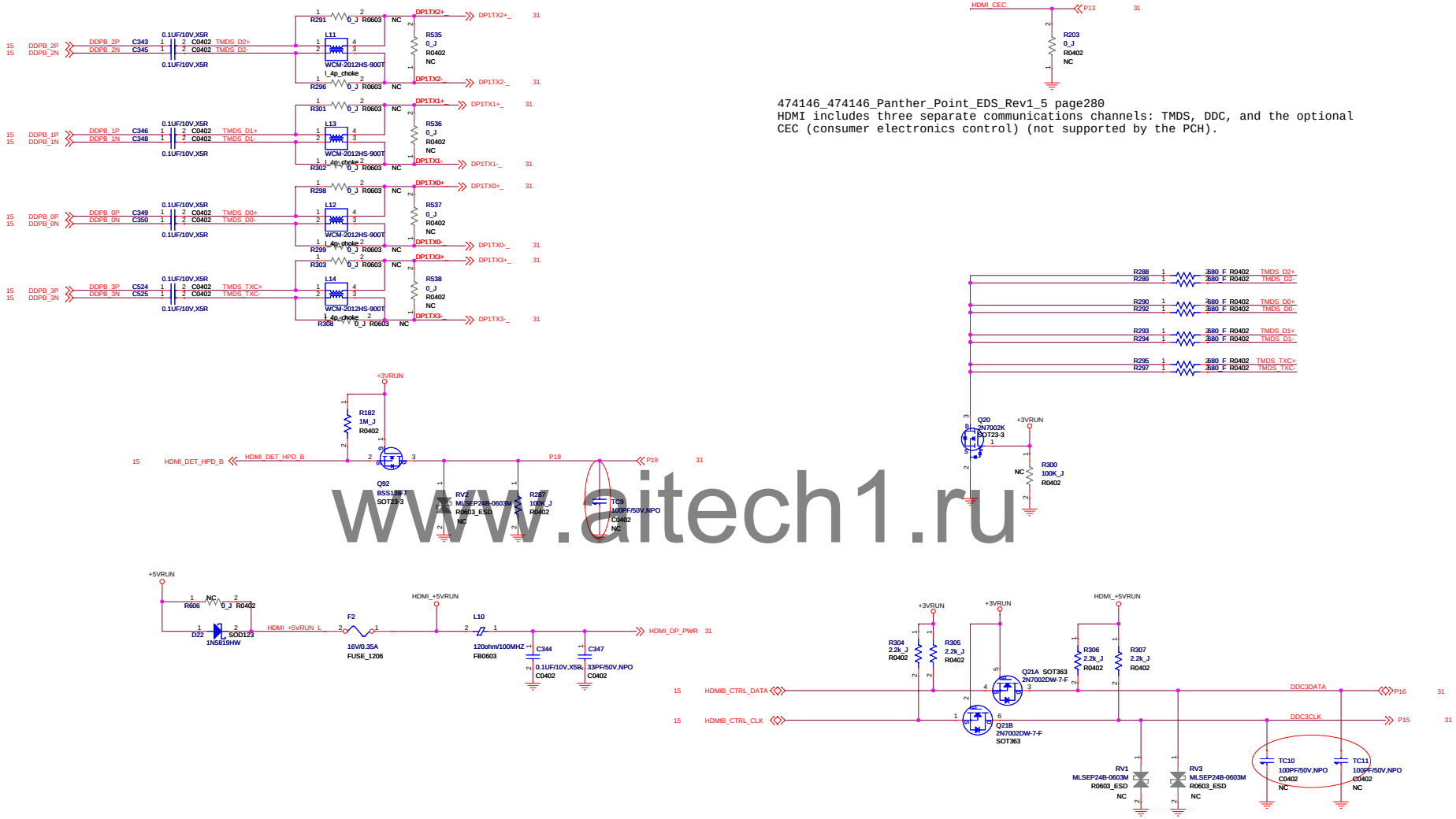

474146_474146_Panther_Point_EDS_Rev1_5 page280
HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) (not supported by the PCH).

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Title: HDMI		
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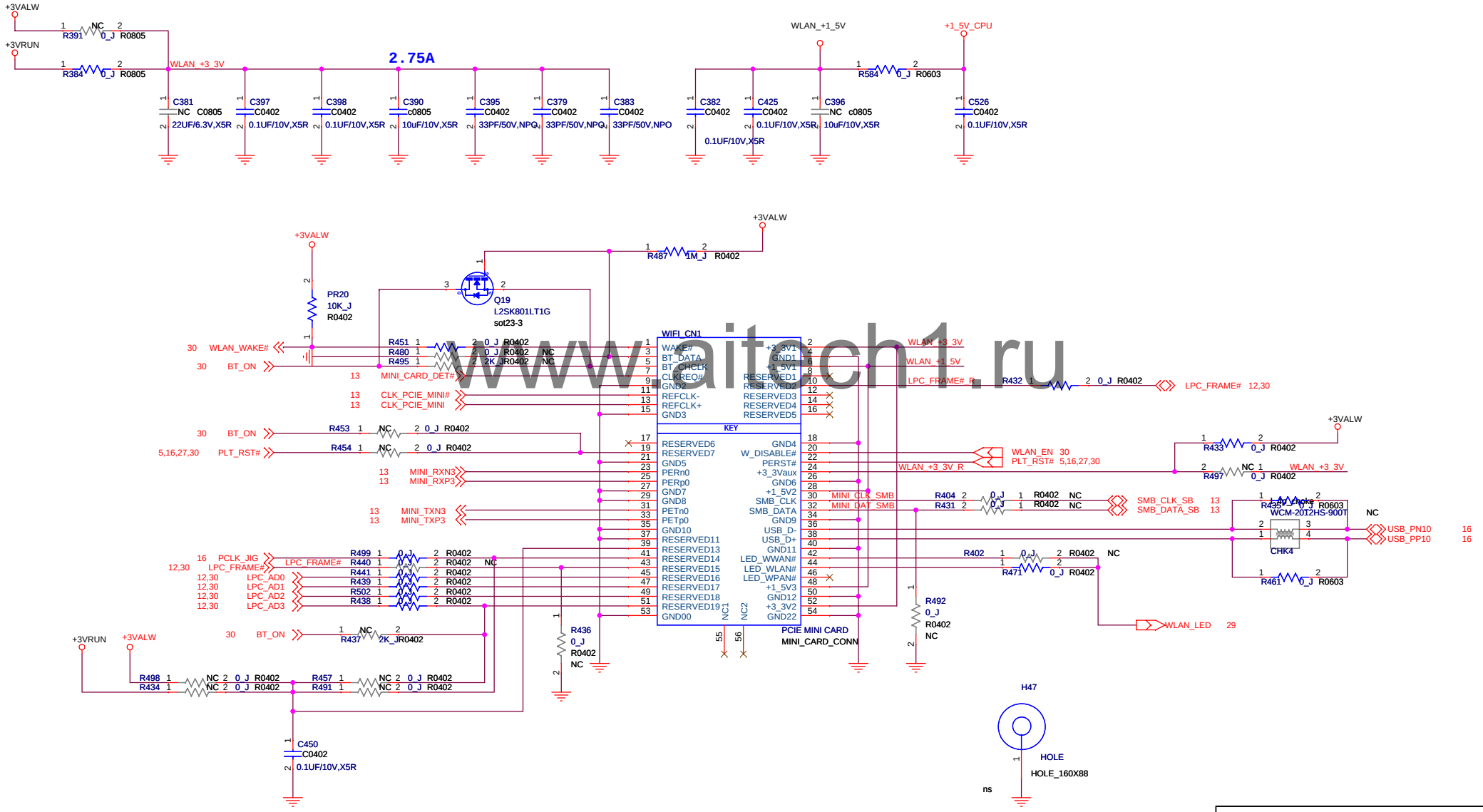

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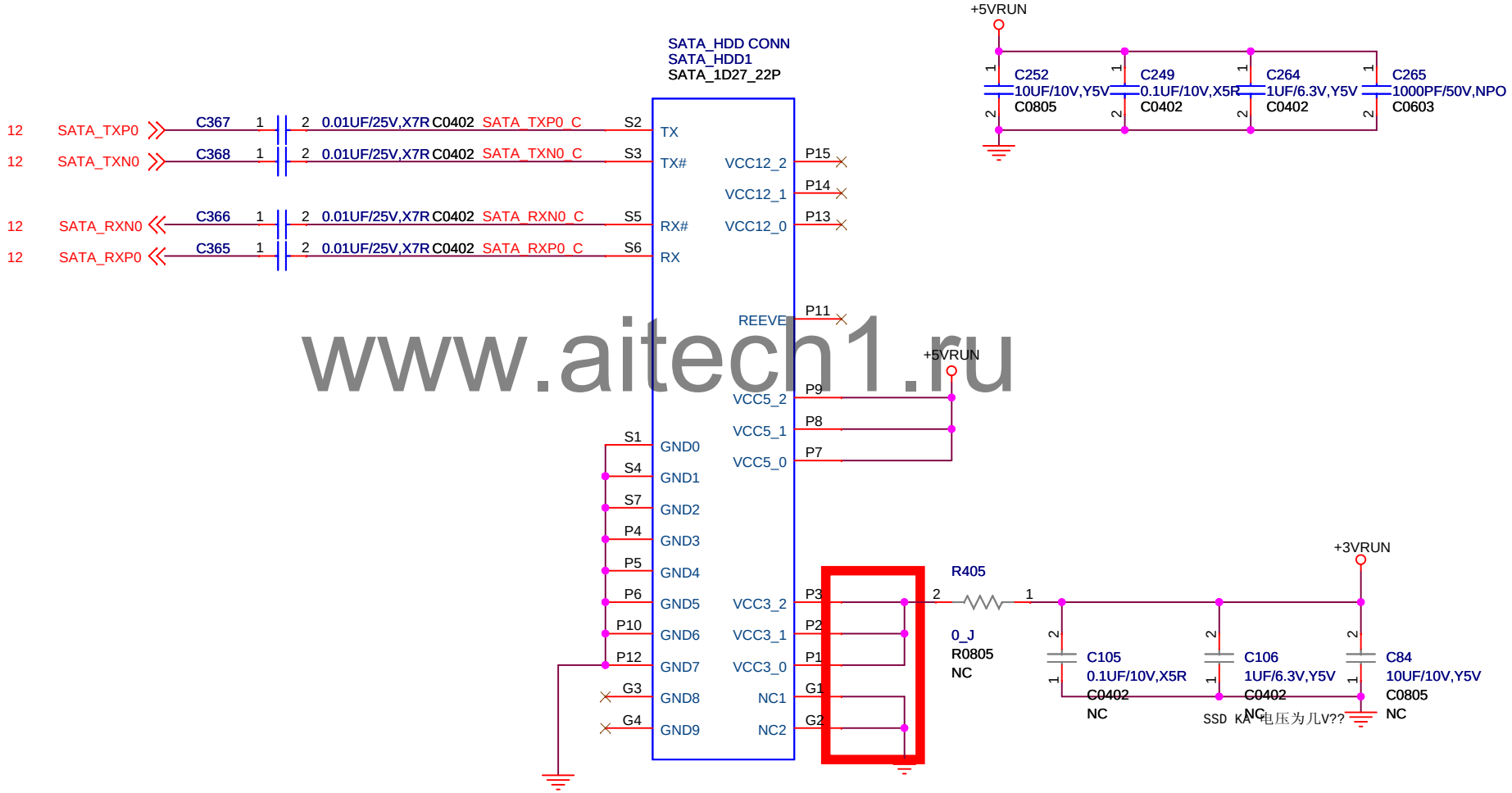

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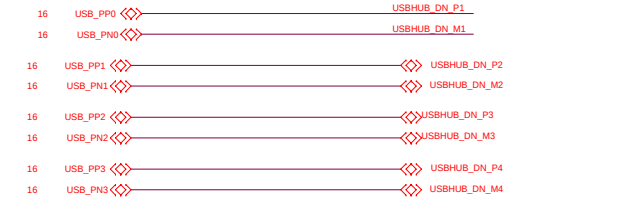
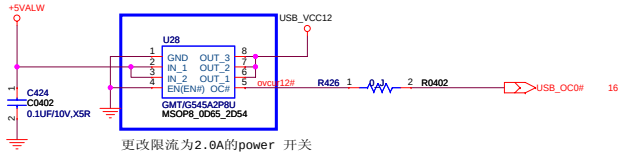
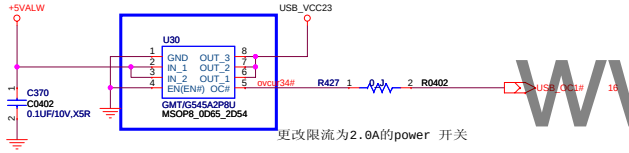
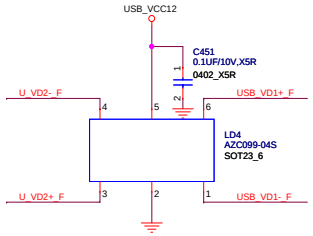


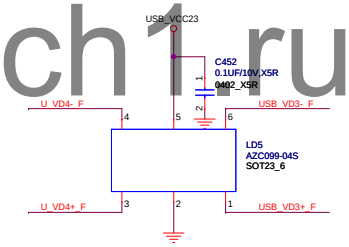


更改限流为2.0A的power 开关

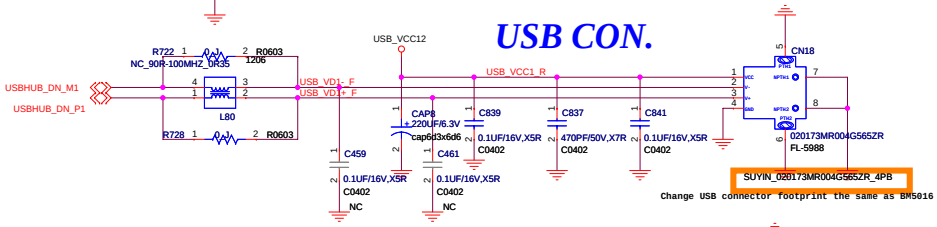


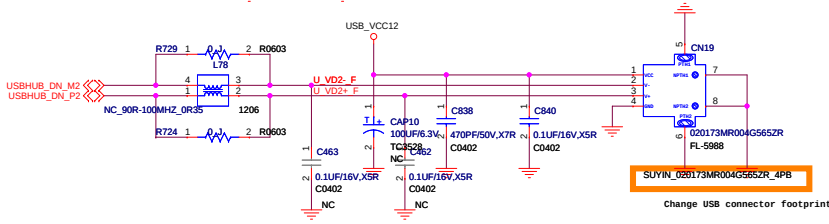
更改限流为2.0A的power 开关

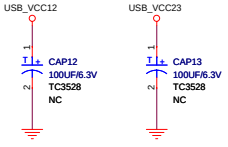




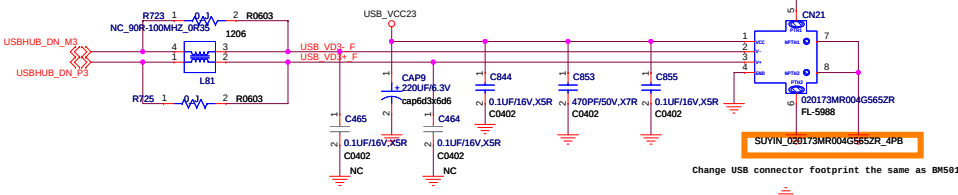
USB CON.







USB CON.



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Title: USB HUB

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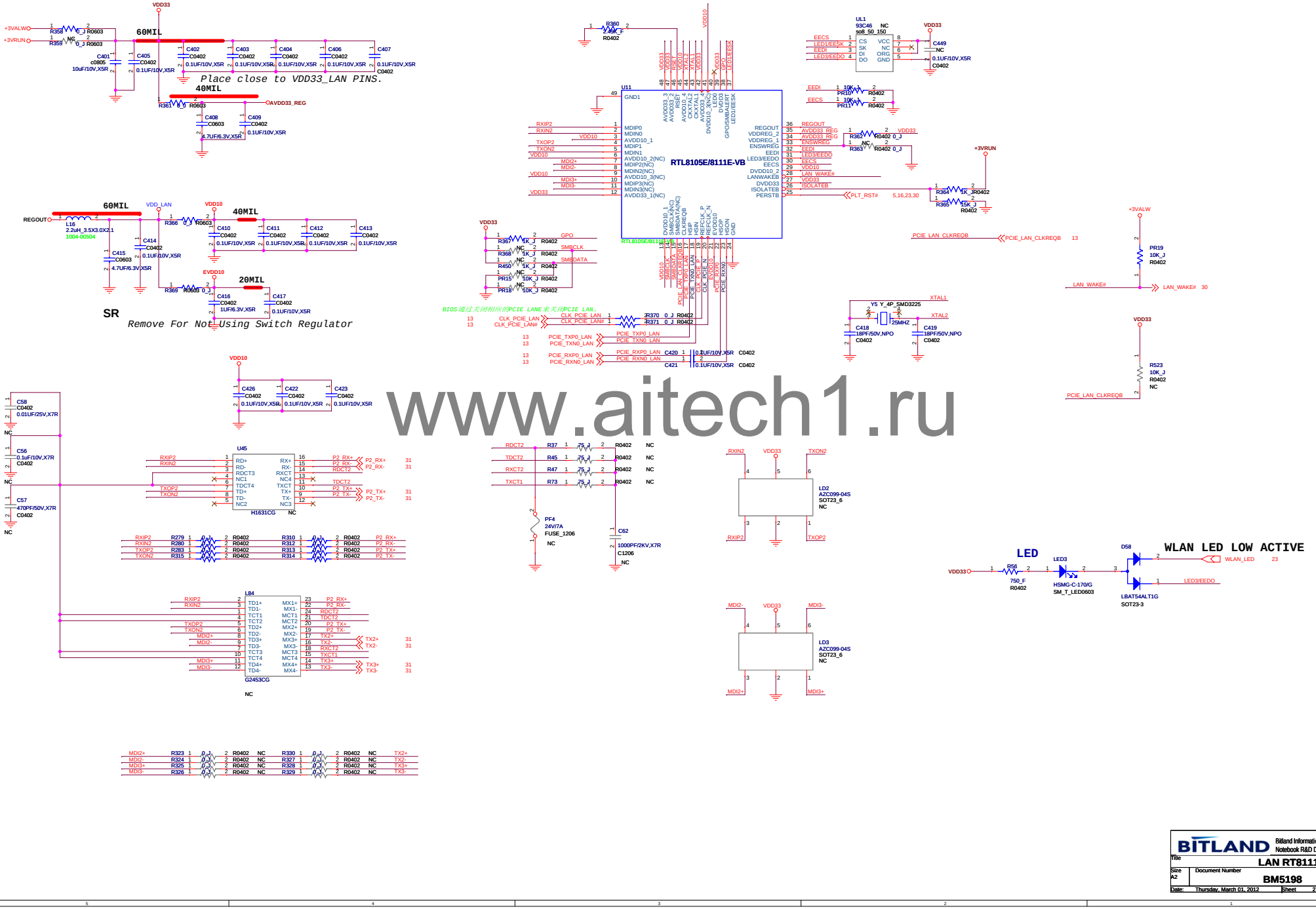

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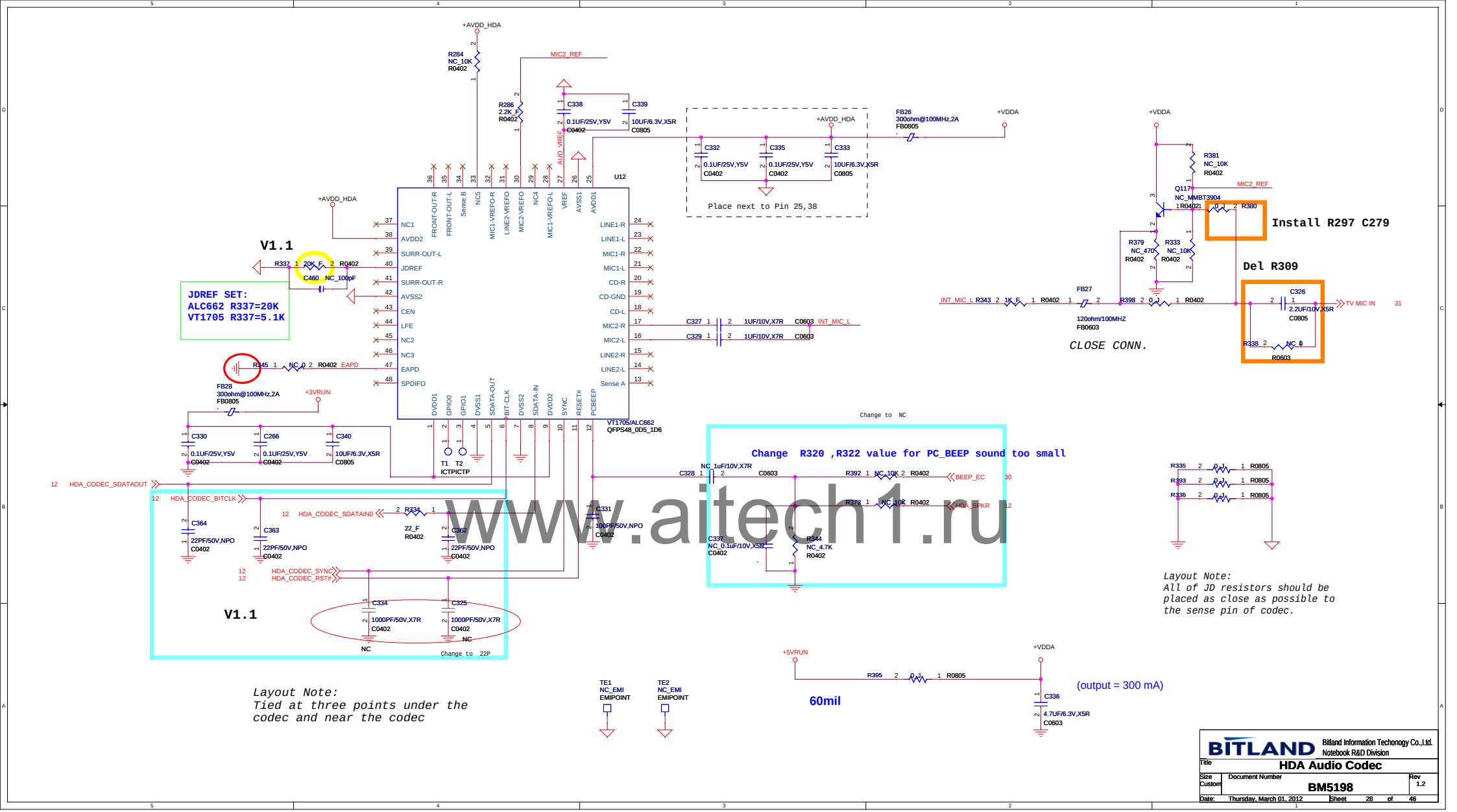

BITLAND	Bitland Information Technongy Co.,Ltd. Notebook R&D Division	
Title: LAN HUB		
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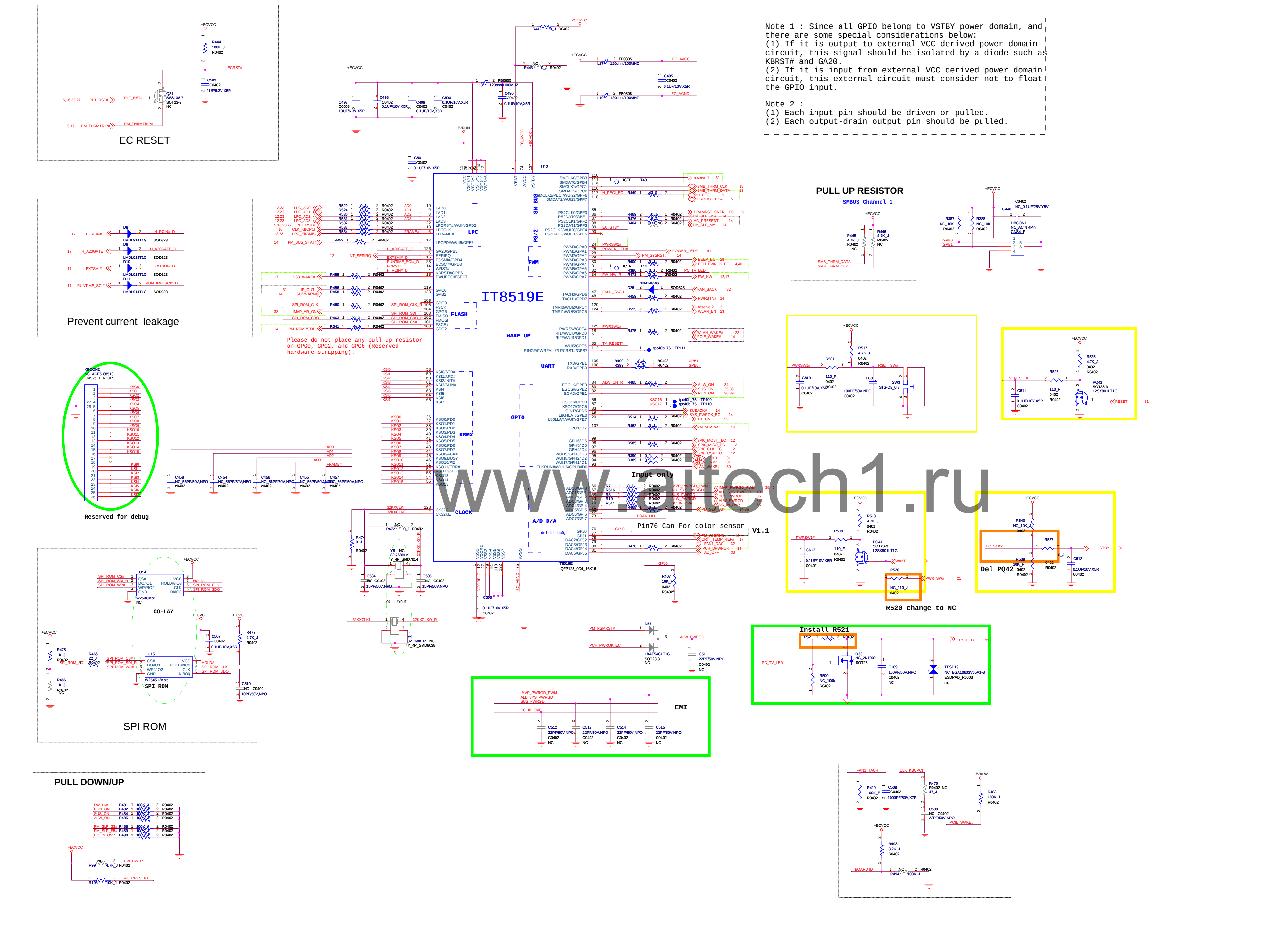
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

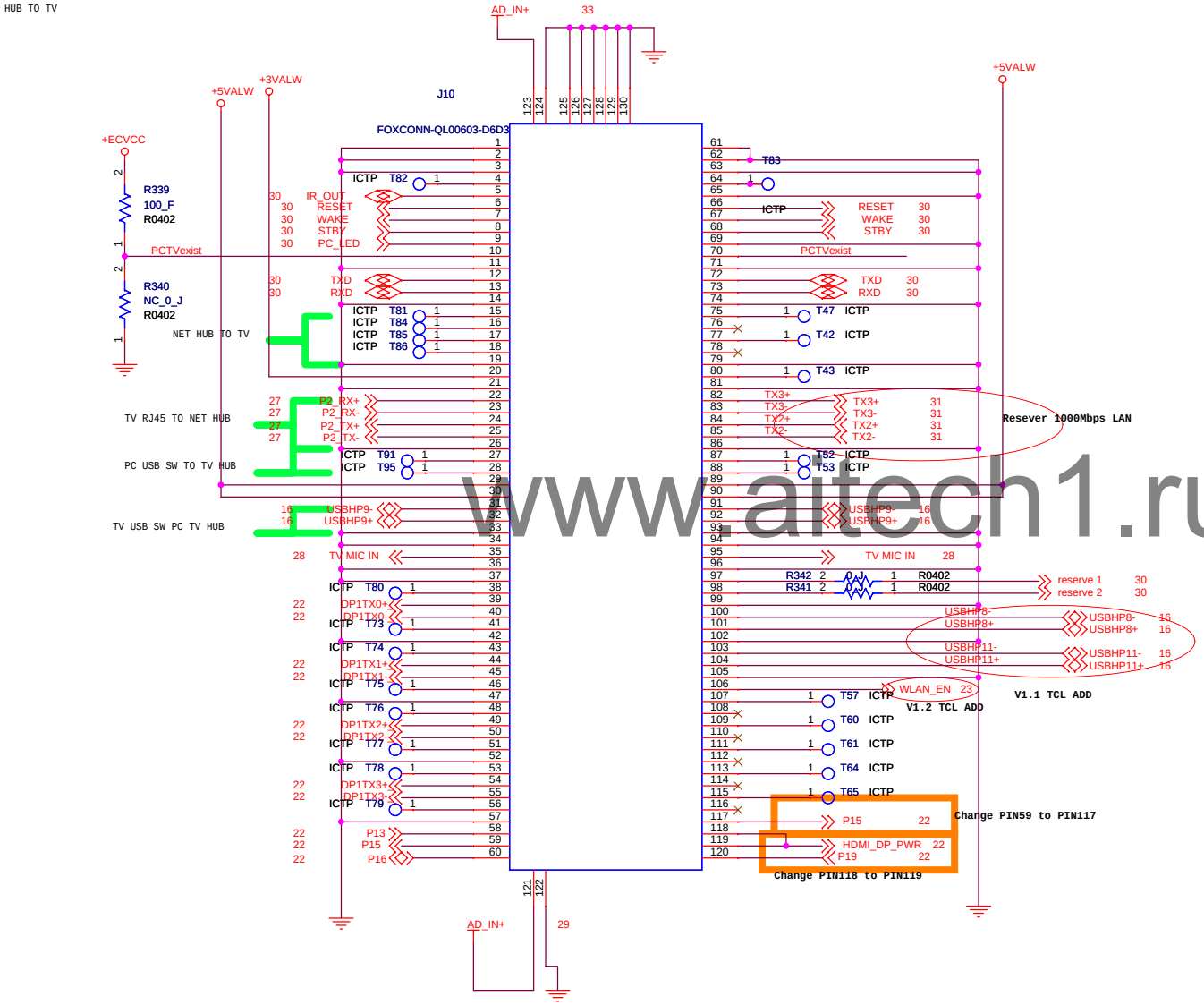


BITLAND Bitland Information Techonogy Co.,Ltd. Notebook R&D Division

Title: EC+KBC(IT8519E)

Size: Custom | Document Number: BM5198 | Rev: 1.2

Date: Thursday, March 01, 2012 | Sheet 30 of 46



	HDMI	DisplayPort
1	TMDS D2+	ML_Lane0+
2	GND Shield	GND
3	TMDS D2-	ML_Lane0-
4	TMDS D1+	ML_Lane1+
5	GND Shield	GND
6	TMDS D1-	ML_Lane1-
7	TMDS D0+	ML_Lane2+
8	GND Shield	GND
9	TMDS D0-	ML_Lane2-
10	TMDS CLK+	ML_Lane3+
11	GND Shield	GND
12	TMDS CLK-	ML_Lane3-
13	CEC	GND
14	Reserved	GND
15	SCL	AUX_CH+
16	SDA	GND
17	DDC/CEC GND	AUX_CH-
18	+5V Power	H.P. Detect
19	H.P. Detect	DP_PWR_Return
20		DP_PWR

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Title	To TV Connector	
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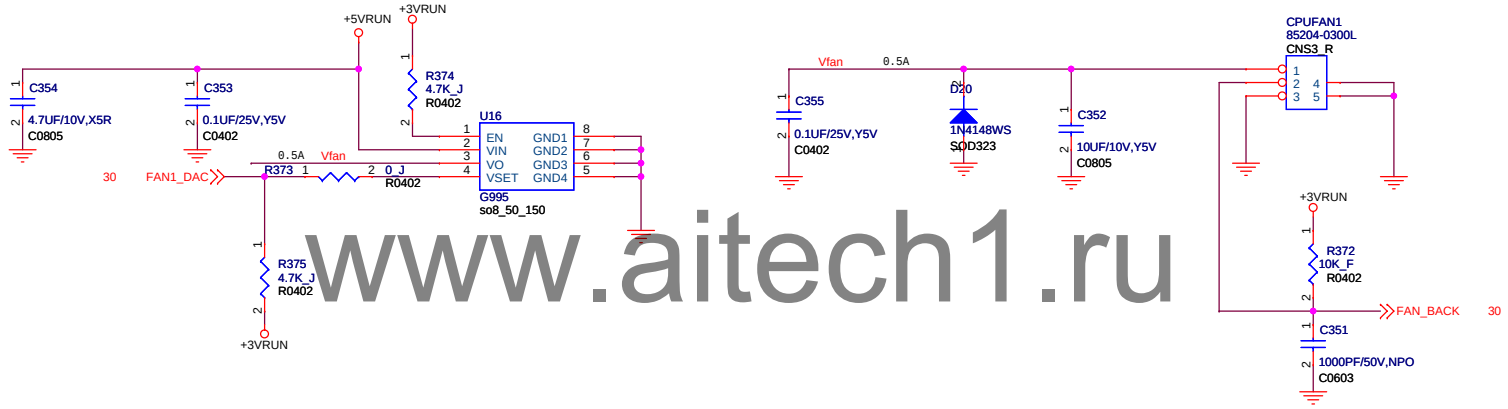
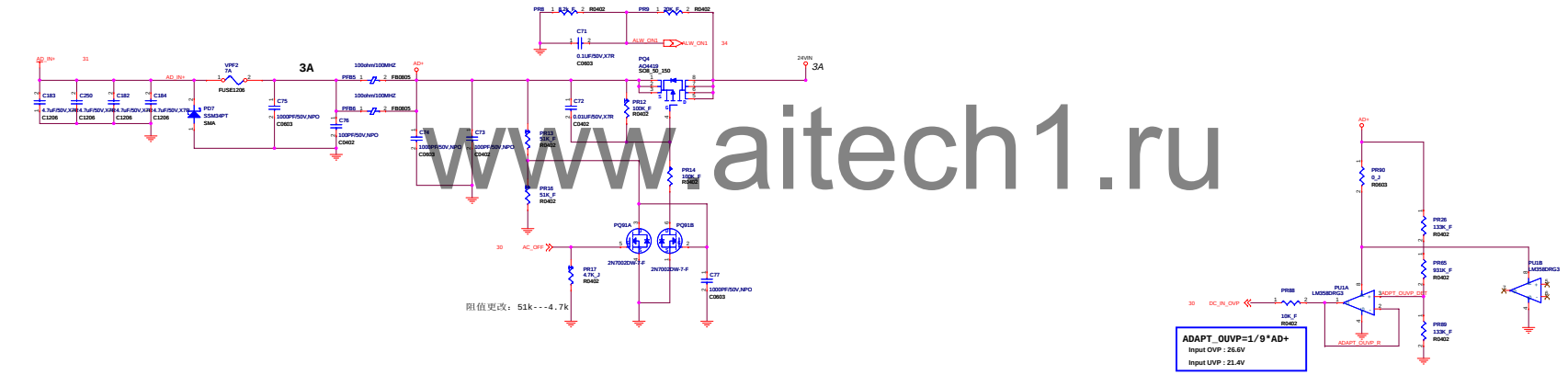
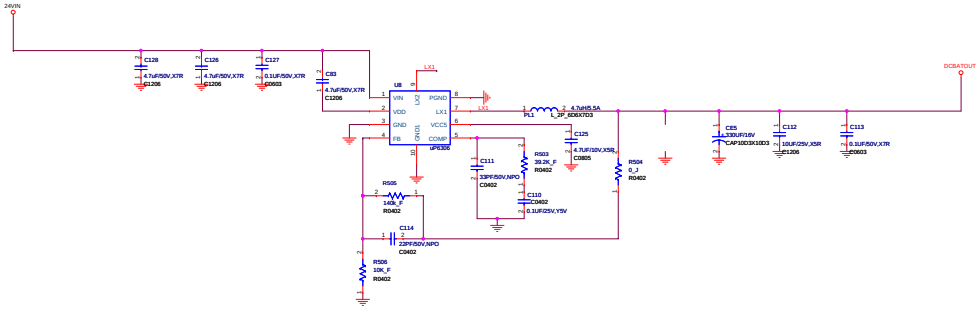
FAN Conn

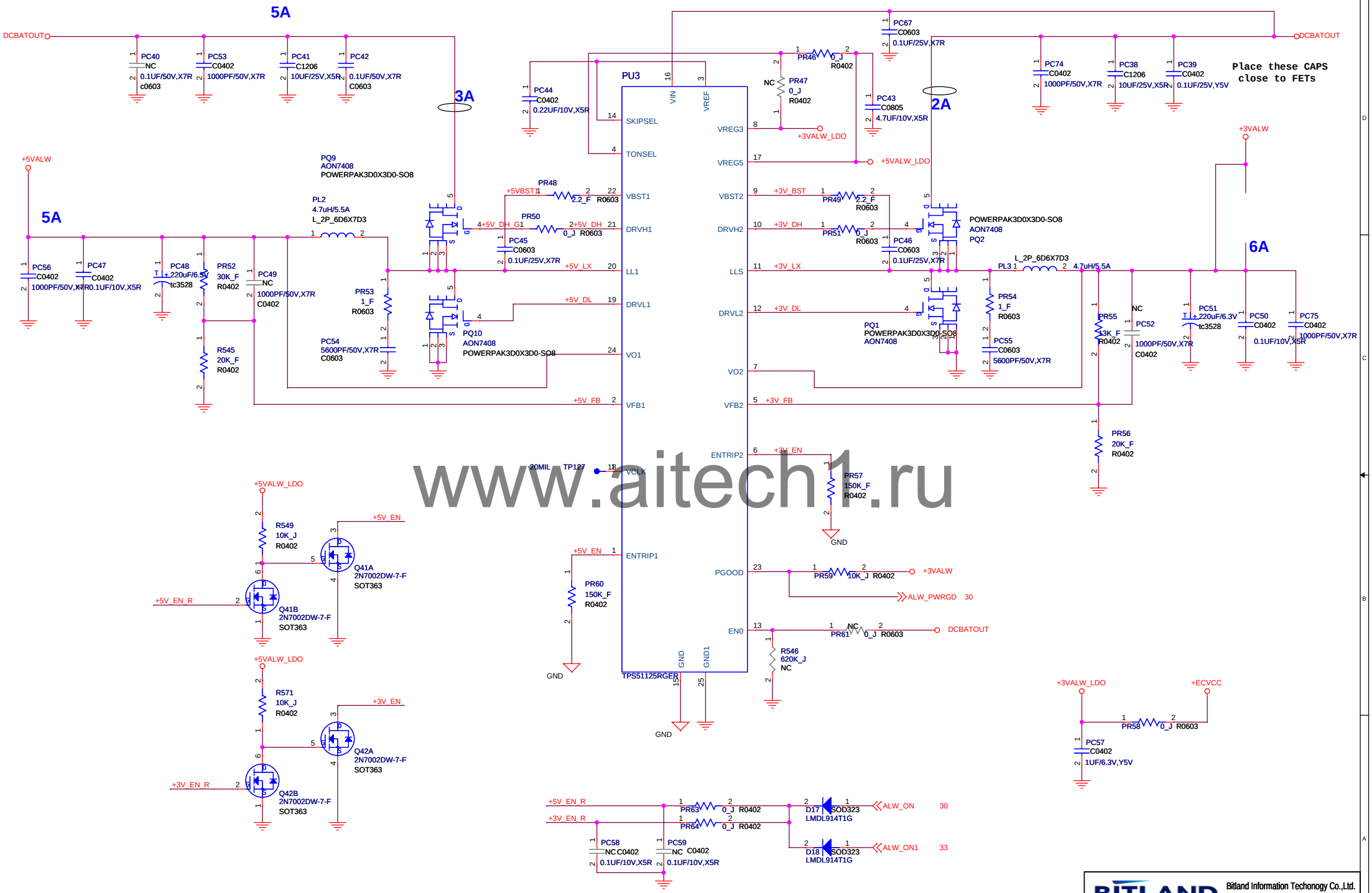


BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	FAN/Thermal Senser	
Size A3	Document Number BM5198	Rev 1.2
Date: Thursday, March 01, 2012	Sheet 32 of 46	





BITLAND	Bitland Information Technology Co.,Ltd. Notebook R&D Division		
Title:	ADAPTER IN&OVP		
Size: A1	Document Number: BM5198		Rev: 1.2
Date: Thursday, March 01, 2012	Sheet 33 of 48		



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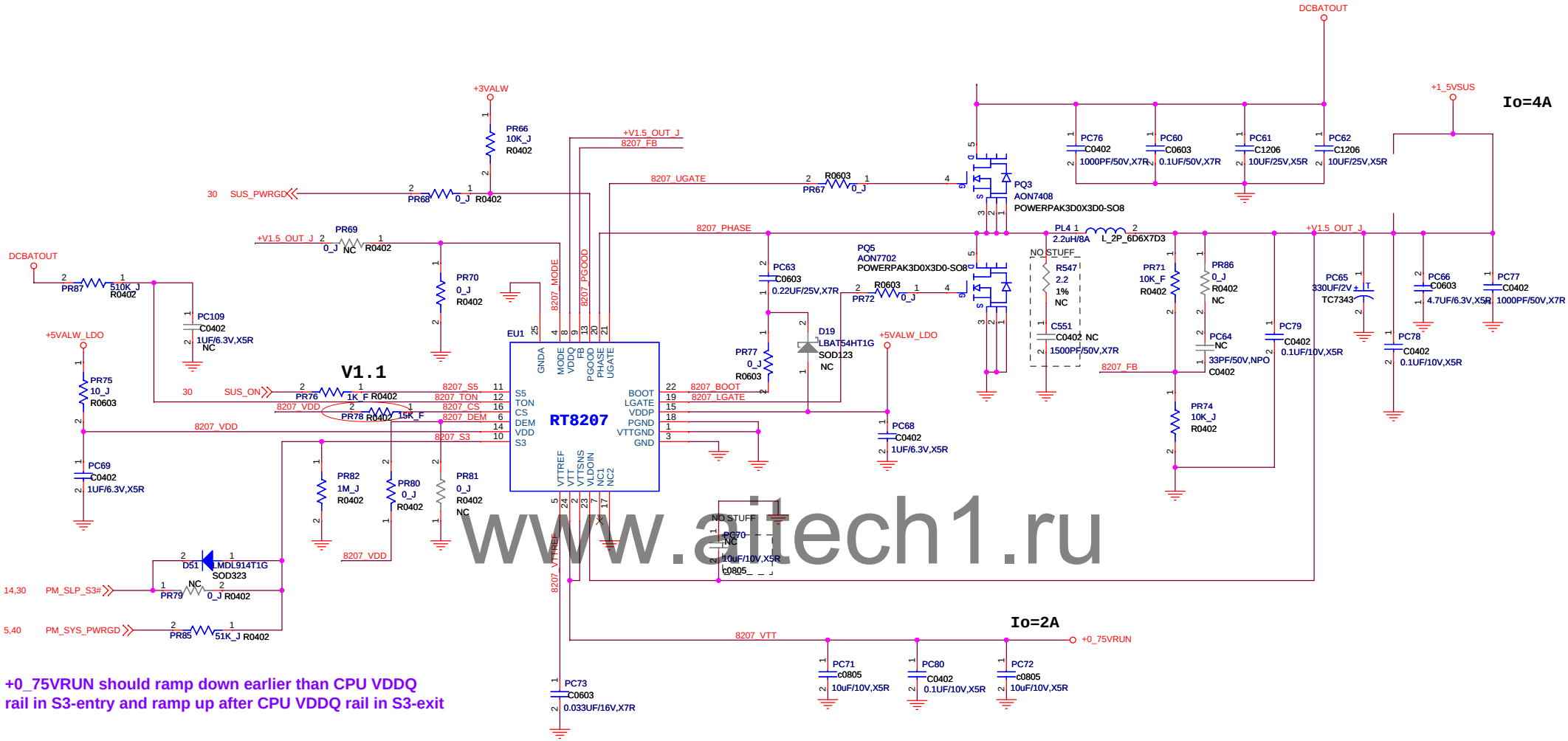
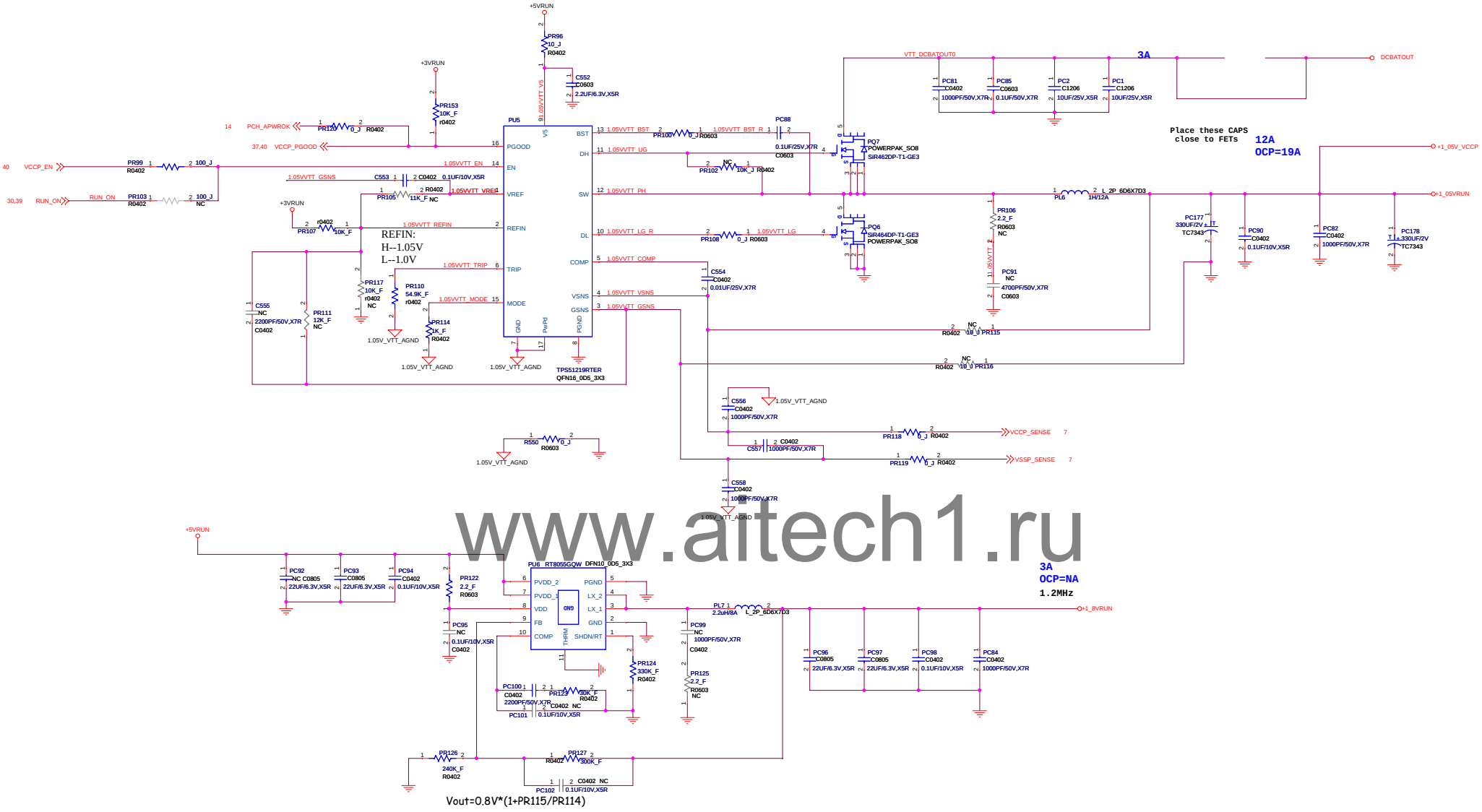
Notebook R&D Division

Title	PWR_+5V/+3V	
Size A3	Document Number BM5198	Rev 1.2
Date: Thursday, March 01, 2012	Sheet 34 of 46	



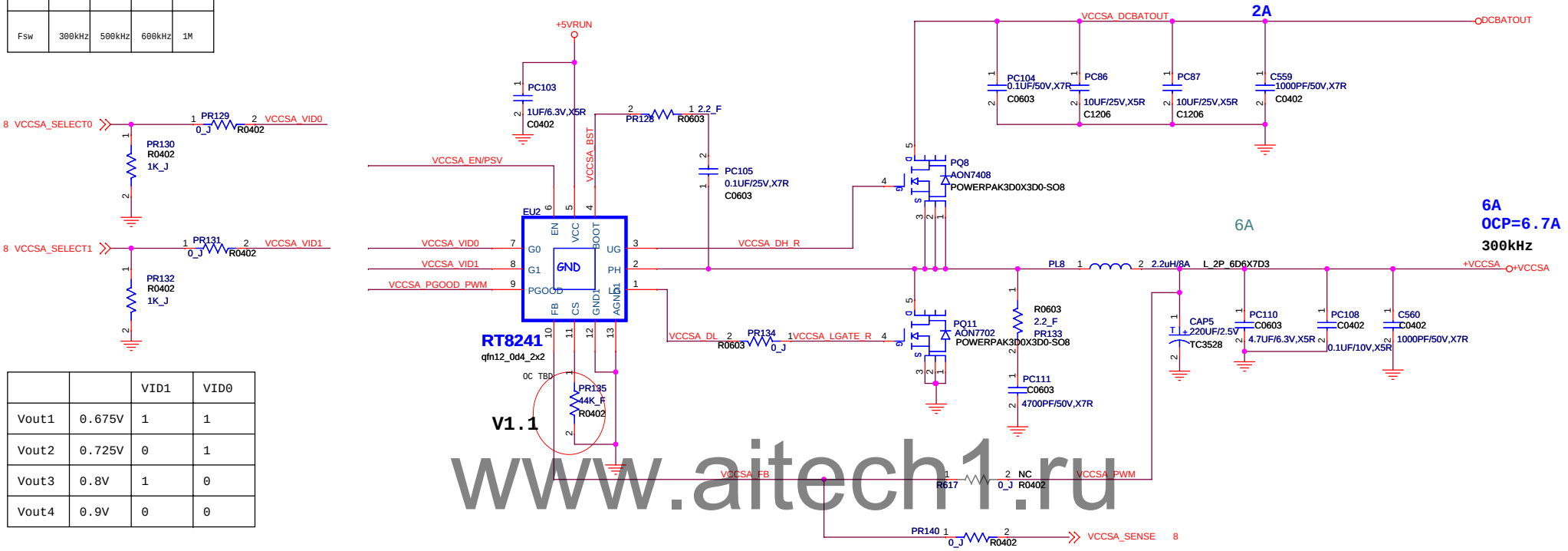
+0_75VRUN should ramp down earlier than CPU VDDQ rail in S3-entry and ramp up after CPU VDDQ rail in S3-exit

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	PWR_+1_5V/+0_75V	
Size A3	Document Number BM5198	Rev 1.2
Date: Thursday, March 01, 2012	Sheet 35 of 46	

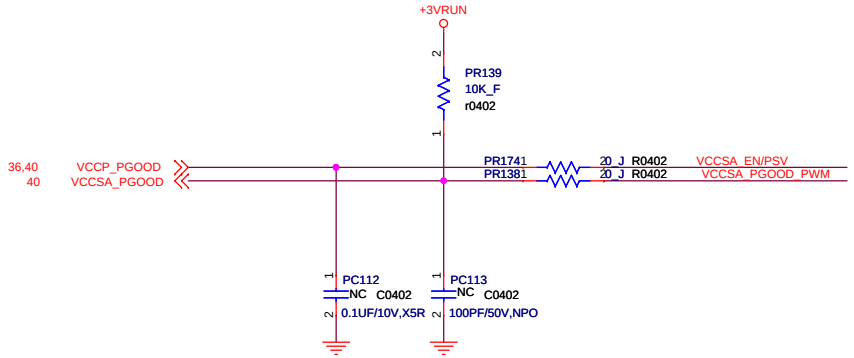


BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	PWR_1.05V_VCCP/1.8V	
Size A2	Document Number BM5198	Rev 1.2
Date: Thursday, March 01, 2012	Sheet 36 of 46	

R140	0	NA	100k	VCC
Fsw	300kHz	500kHz	600kHz	1M



		VID1	VID0
Vout1	0.675V	1	1
Vout2	0.725V	0	1
Vout3	0.8V	1	0
Vout4	0.9V	0	0



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Notebook R&D Division

Title	PWR_VCCSA	
Size A3	Document Number BM5198	Rev 1.2
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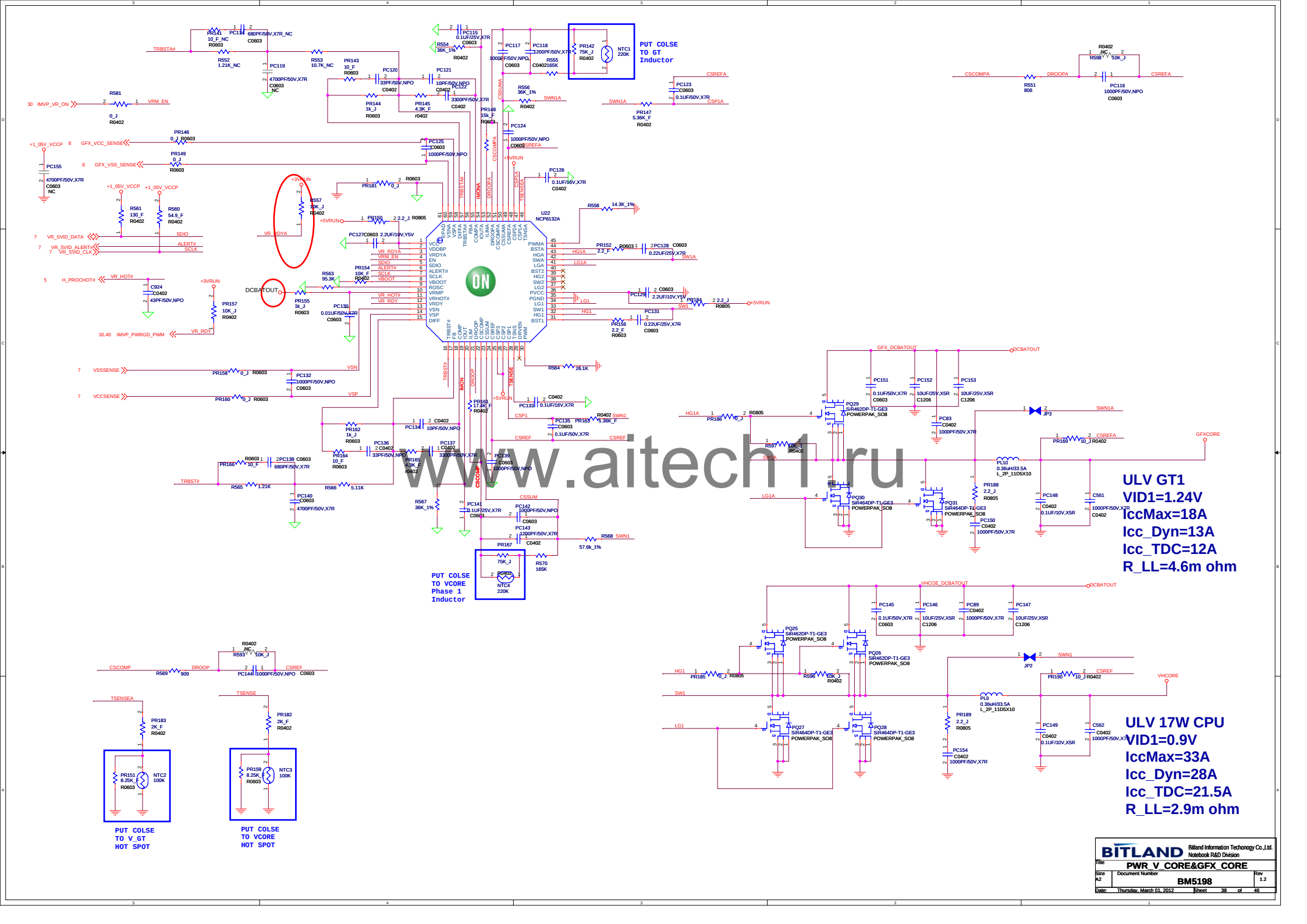

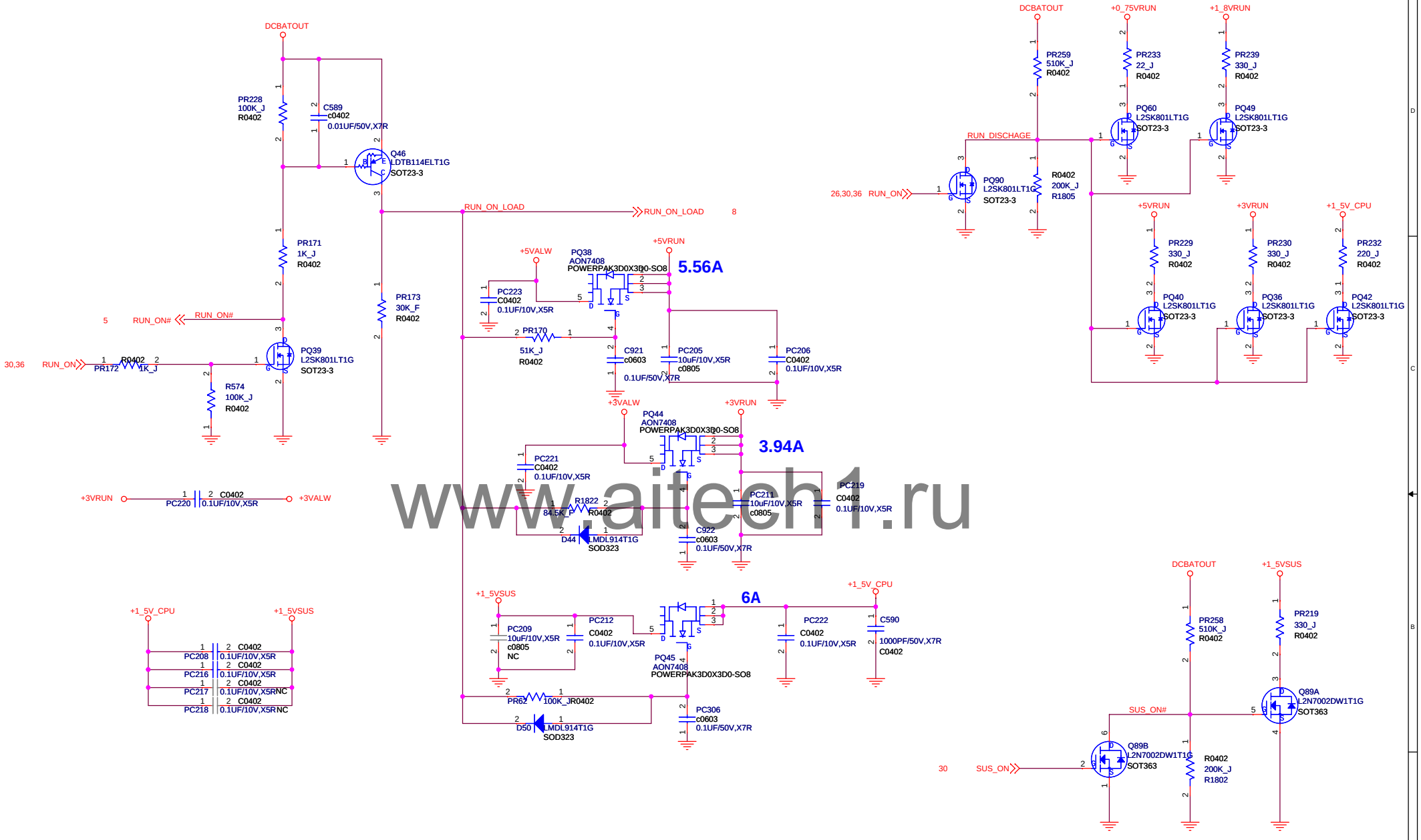

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Notebook R&D Division

Title: PWR_Others power plane

Size	Document Number	Rev
A3	BM5198	1.2

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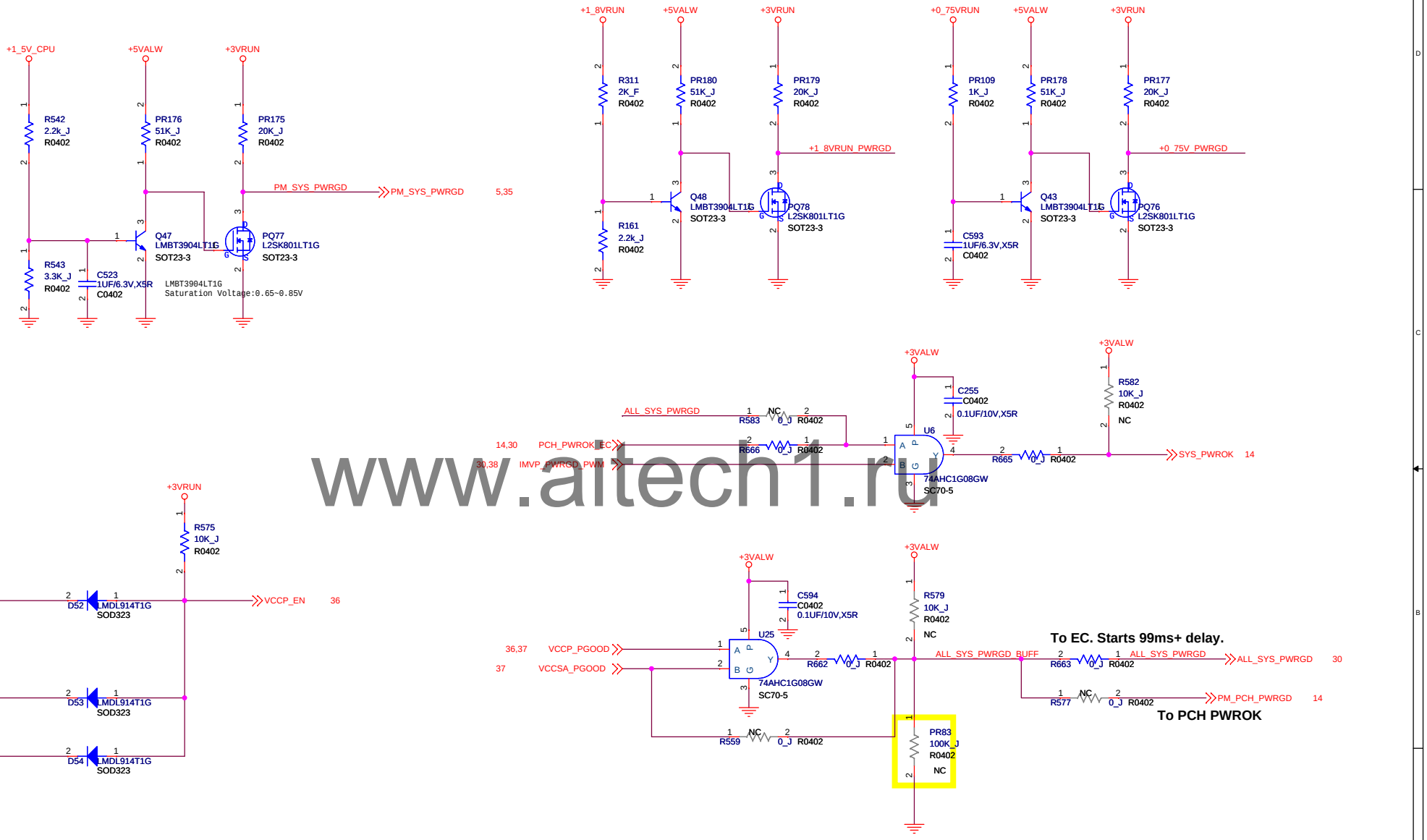

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Power Sequence Logic	
Size A3	Document Number BM5198	Rev 1.2
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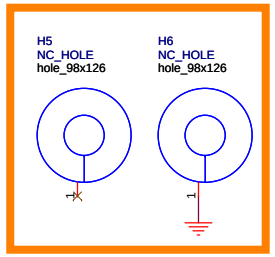
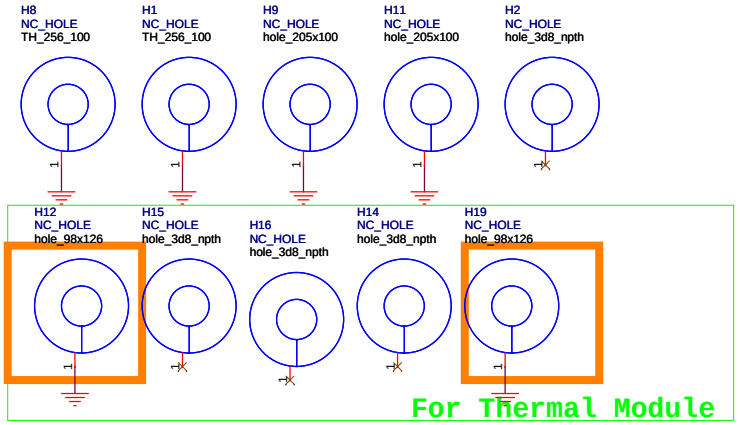
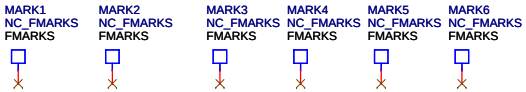
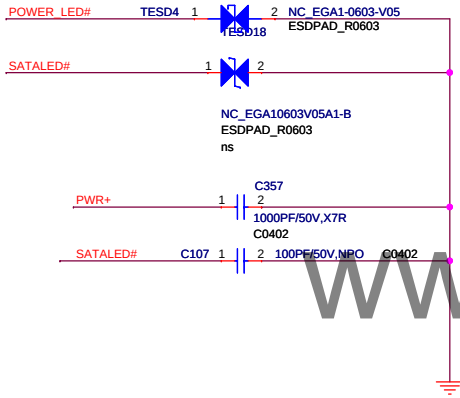


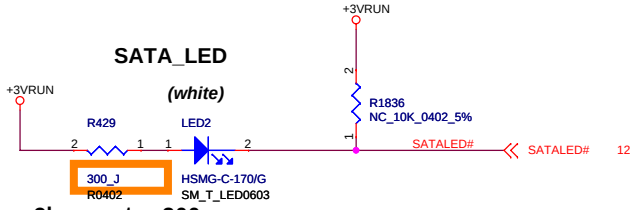
H5 H6 H12 H19 FOOTPRITN change to hole_98x126



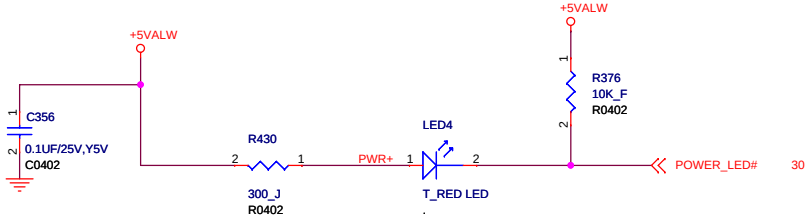


HOLE/MARK





Change to 300



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Title: HOLE		
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Voltage Rails

Power Plane	Description	S1	S3	S5
DC_IN	Adapter power supply (19V)	N/A	N/A	N/A
DCBATOUT	AC or battery power rail for power circuit.	N/A	N/A	N/A
+V_CORE	Core voltage for CPU	ON	OFF	OFF
+0_75V	0_75VRUN LDO power rail for DDR terminator	ON	OFF	OFF
+1_05VRUN	1.05V switched power rail	ON	OFF	OFF
+5VRUN	5V switched power rail	ON	OFF	OFF
+1_5VSUS	1.5V power rail for DDR	ON	ON	OFF
+1_5VRUN	1.5V switched power rail	ON	OFF	OFF
+1_8VRUN	1.8V power rail for system	ON	OFF	OFF
+1_5V_CPU	1.5V switched power rail	ON	OFF	OFF
+1.05V_VCCP	VCCP switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VSUS	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VRUN	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VSUS	5V switched power rail	ON	ON	OFF
PEX_VDD	PEX LDO power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+VCCSA	SA voltage for CPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
MEDIA CONSOLE	1010 000X b

EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b
NB9M THERMAL SENSOR	

HM55 SM Bus address

Device	Address
Clock Generator (SLG8SP587V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*SUS	+V*RUN	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	1.0
2	1.1
3	1.2
4	1.3
5	
6	
7	

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Title: NOTE LIST

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VER1.1----2/9
1,Q34 NC;R74上件----WLAN LED Low active
2, RT8241DZQW改为RT8241F----for Vccsa
3,SATA---G1、G2的螺丝加丝印位置；Docking----Pin129,、130的螺丝加丝印位置
1101-00102 SATA连接器螺丝
1101-00034 Docking螺丝
4,R176上件,要enable
5,HDMI Data0和2交换
6,VT1705换为ALC662; R337改为20K
7，C334、C325 NC;
8, PR78=7.68k改成15k;PR135=22K改成44K---Power要求，修改OCP
9, 装配图中C294与C290位置对调---layout装配图错误,需修改
10，工厂建议USB接口改SMT，将USB插件孔加大,比元件脚大0.1~0.2mm左右,
11，LVDS disable：R319 NC,R320上件；L2 NC，PR191上件,删除C360、C373、C378
12,删除PJ点
13,TCL要求：在PC盒增加两路USB信号输入（1路给遥控接收，1路预留给WiFi)
14,change clk_RUN# to ec 77pin
EMI修改:
1,增加R603
2,HDMI预留bridge
3,HDMI DDC & DET预留100pF到地
5，HDMI上90Ohm common choke
6，在USB连接器CN18/CN19/CN20/CN21端的USB的差分线预留bypass电容位置，正负各留一颗。

VER1.2-----2/28
1,删除LAN switch部分线路，删除120PIN的15、16、17、18脚（connect to TV LAN）
2,保留100M的LAN（120PIN的22、23、24、25脚），1000M的LAN不做预留了。
3,删除120PIN的80脚LED_2_LAN
4,将WIFI插座的wlan en脚连到120PIN的106脚
5,删除usb hub部分线路（删除120PIN的27、28、87、88脚PC USB SW TO TV HUB），将4路USB信号直接进PC的pch

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	History and Changelist	
Size A3	Document Number BM5198	Rev 1.2
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